ZD25WQ32C

Ultra Low Power, 32M-bit

Serial Multi I/O Flash Memory Datasheet

Performance Highlight

- Wide supply range from 1.65V to 3.6V for Read, Erase and Program
- Ultra-Low Power consumption for Read, Erase and Program
- x1, x2 and x4 Multi I/O Support
- High reliability with 100K cycling endurance and 20-year data retention
- Page/Sector/Block Erase
- Fast Chip Erase time 10ms

ZETTA Technology, Inc.

Contents

1. OVERVIEW

The ZD25WQ32C (32M-Bit) serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI : Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#).

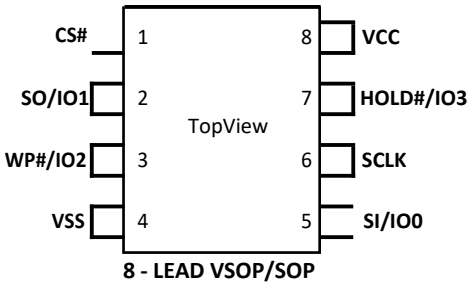
The Dual I/O & Dual output data is transferred with speed of 208Mbits/s and the Quad I/O & Quad output data is transferred with speed of 416Mbits/s.

Specifically designed for use in many different systems, the device supports read, program, and erase operations with a wide supply voltage range of 1.65V to 3.6V. No separate voltage is required for programming and erasing.

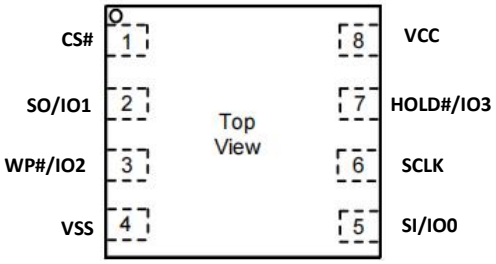
1.1 Performance

- **SPI Flash Memories**
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
  - Quad SPI： SCLK, CS#, IO0, IO1, IO2, IO3
- **Highest Performance Serial Flash**
  - 1 IO 104MHz for fast read
  - 2 IO Dual I/O Data transfer up to 208Mbits/s
  - 4 IOQuad I/O Data transfer up to 416Mbits/s
- **Power Supply and Low Power Consumption**
  - Single 1.65V to 3.6V supply
  - 7μA standby current,0.2μA deep power down current
  - 2.0mA active read current at 33MHz,2.0mA active program or erase current
- **Flexible Architecture**
  - Uniform 256-byte Page Erase,Uniform 4K-byte Sector Erase
  - Uniform 32/64K-byte Block Erase,Program 1 to 256 byte per programmable page
  - Minimum 100,000 Program/Erase Cycles,More than 20-year data retention
- **Fast Program and Erase Speed**
  - 2.0ms page program time,10ms page erase time
  - 10ms 4K-byte sector erase time,10ms 32K/64K-byte block erase time
- **Advanced Security Features**
  - 128-Bit Unique ID for each device
  - 3*1024-Byte Security Registers with OTP Locks
  - Discoverable parameters (SFDP) register
- **Package Information**
  - SOP8(150MIL/208MIL),TSSOP-8(173MIL)
  - USON-8(2*3mm)
  - Contact ZETTA for KGD and other options

1.2 Pin Definition



8 - LEAD VSOP/SOP



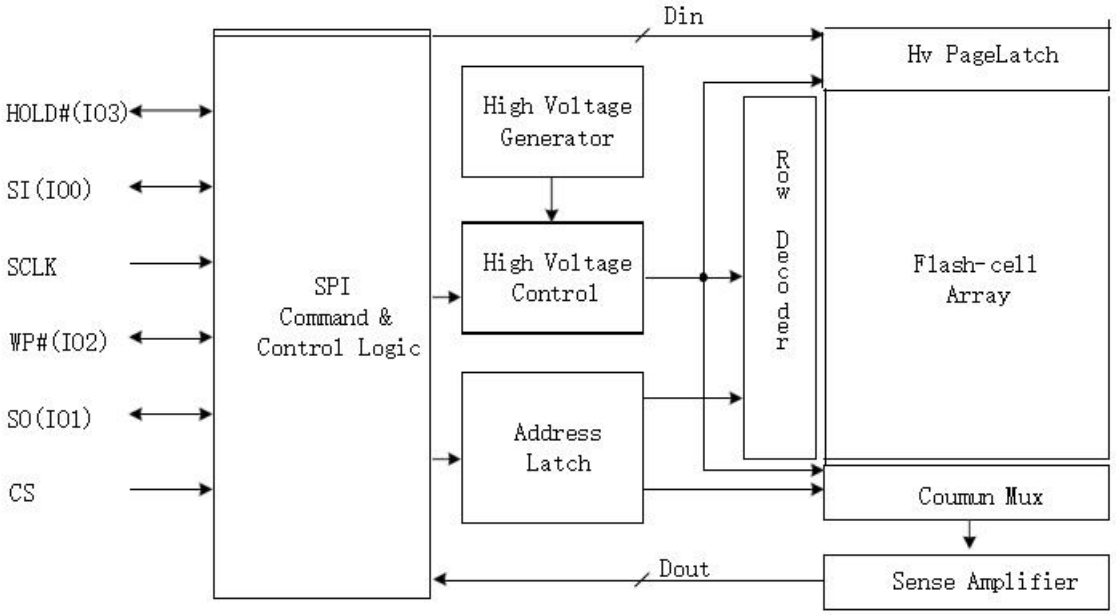
8 - LEAD WSON/USON

Table-1. Pin Definition

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
8	VCC		Power Supply

2. DESCRIPTION

2.1 Block diagram



2.2 Memory organization

Table-2. ZD25WQ32C Array Organization

Each device has	Each block has	Each sector has	Each page has	
4M	64/32K	4K	256	Bytes
16K	256/128	16	-	Pages
1024	16/8	-	-	Sectors
64/128	-	-	-	Blocks

Table-3. ZD25WQ32C Uniform Block Sector Architecture

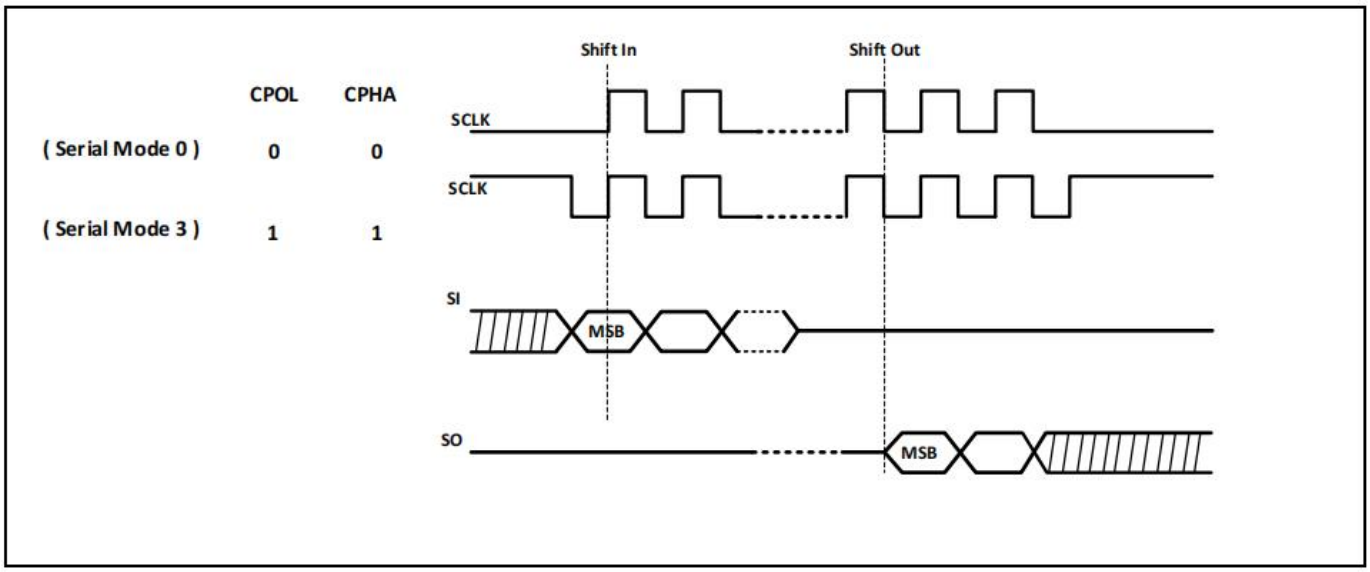
Block	Sector	Address range	
63	1023	3FF000H	3FFFFFH
	.....	.....	.....
	1008	3F0000H	3F0FFFH
62	1007	3EF000H	3EFFFFH
	.....	.....	.....
	992	3E0000H	3E0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

3. DEVICE OPERATION

3.1 Mode0 and Mode3

1. Before a command is issued, the status register should be checked to ensure the device is ready for the intended operation.
2. When an incorrect command is input, the device enters standby mode and remains in standby mode until the next CS# falling edge. In standby mode, the SO pin of the device is in High-Z.
3. When the correct command is input, the device enters active mode and remains in active mode until the next rising edge of CS#.
4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference between Serial mode 0 and mode 3 is shown in Figure-1.

Figure-1. Serial Modes Supported (for Normal Serial Mode)



Standard SPI

The ZD25WQ32C features a serial peripheral interface on 4 signals: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and is data shifted out on the falling edge of SCLK.

Dual SPI

The ZD25WQ32C supports Dual SPI operation when using the “Dual Output Fast Read” (3BH), “Dual I/O Fast Read” (BBH) , “Dual I/O Read Manufacture ID & Device ID” (92H) and “Dual Input Page Program” (A2H) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

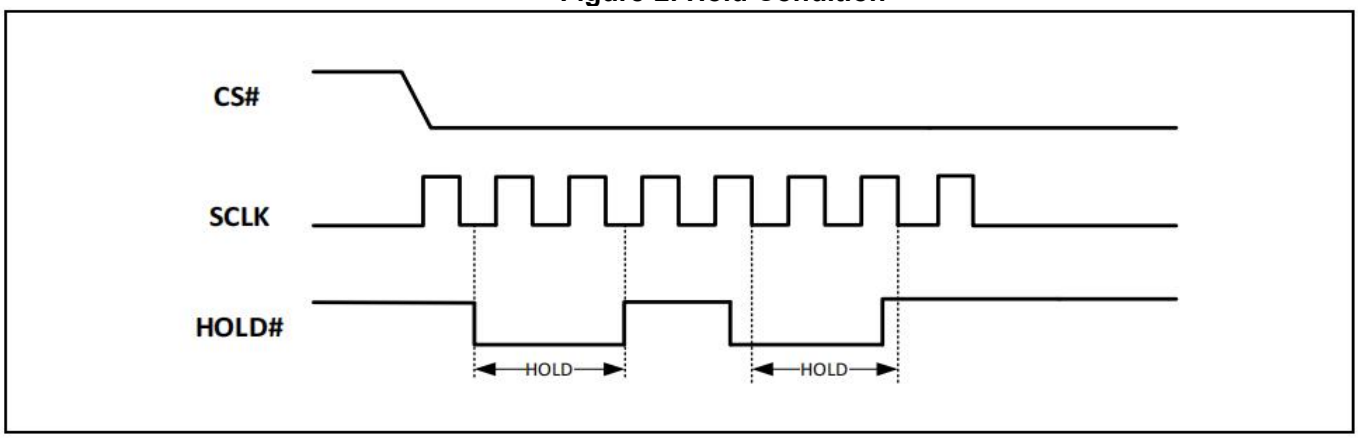
The ZD25WQ32C supports Quad SPI operation when using the “Quad Output Fast Read” (6BH), “Quad I/O Fast Read” (EBH/E7H/E3H), “Quad I/O Read Manufacture ID/Device ID” (94H) and “Quad Input Page Program” (32H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command, the SI, SO, WP# and HOLD# pins become bidirectional I/O pins: IO0, IO1, IO2 and IO3, respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

Hold

Driving the HOLD# pin low will pause any serial communications with the device. The HOLD feature will not stop the following operations if already in progress when the HOLD# pin goes low: status register write, program, or erase.

The operation of HOLD requires Chip Select (CS#) to remain low and begins on the falling edge of HOLD# pin signal while the Serial Clock (SCLK) signal is low (if the Serial Clock signal is not low, the HOLD operation will not start until the Serial Clock signal is low). The HOLD condition ends on the rising edge of HOLD# pin signal while the Serial Clock (SCLK) signal is low (if the Serial Clock signal is not low, the HOLD operation will not end until the Serial Clock is low).

Figure-2. Hold Condition



During the HOLD operation, the Serial Data Output (SO) is in a high impedance state when the HOLD# pin goes low and will remain in a high impedance state until the HOLD# pin goes high. The Serial Data Input (SI) is ignored (don't care) if both the Serial Clock (SCLK) and HOLD# pin go low and will remain in this state until the SCLK goes low and the HOLD# pin goes high. If Chip Select (CS#) is driven high during the HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be driven high and CS# must be at a logic low.

Note: The HOLD feature is disabled in Quad I/O mode.

3.2 STATUS REGISTER AND CONFIGURATION REGISTER

Table-4. Status Register

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1
Read-only	Non-volatile	Non-volatile OTP			Read-only	Non-volatile	Non-volatile

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Non-volatile	Non-volatile					Read-only	Read-only

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the device is busy executing a program/erase/write status register operation. When the Write in Progress (WIP) bit is set to 1, a program/erase/write status register operation is in progress. When the Write in Progress (WIP) bit is set to 0, the device does not have a program/erase/write status register operation in progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset, and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area software protected against Program and Erase commands. These bits are written with the Write Status Register (01H) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to the target value, the relevant memory area (as defined in Table-7.X) becomes protected against Page Program (02H), Page Erase (81H), Sector Erase (20H), Half Block Erase (52H) and Block Erase (D8H) commands. The Chip Erase (60H or C7H) command is executed, only if the Block Protect bits are set to “None protected”. The Block Protect bits can be written if the Hardware Protection Mode has not been set.

SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection.

Table-5. Status Register Protection Bits

SRP1	SRP0	#WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
0	1	0	Hardware Protected	WP#=0, the Status Register is locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down (1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program (2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact ZETTA for details.

QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the device is set to Standard SPI operation and both WP# and HOLD# pins are enabled. When the QE bit is set to 1, the Quad IO2 and IO3 pins are enabled and the WP# pin function is not available since this pin is used for IO2. (Set the QE bit to 0 to avoid short issue if the WP# or HOLD# pin is tied directly to the power supply or ground.)

LB3, LB2, LB1 bits

The LB3, LB2, LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status for the Security Registers. The default state of LB3-LB1 is 0, with the security registers unprotected. The LB3-LB1 bits can be set to 1 individually using the Write Register (01H or 31H) command. The LB3-LB1 bits are One Time Programmable, once setting to 1, the corresponding Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the memory array protection. Please see the Table-7.X for protect area details. The default setting is CMP=0.

SUS1, SUS2 bit

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing a Program/Erase Suspend (75H or B0H) command. (The Erase Suspend will set the SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by the Program/Erase Resume (7AH or 30H) command, the Software Reset (66H+99H) command as well as a power-down, power-up cycle.

3.3 Configuration Register (CR)

Table-6. Status Register

C7	C6	C5	C4	C3	C2	C1	C0
Reserved	**DRV1**	**DRV0**	**QP**	**Reserved**	**Reserved**	**Reserved**	**DC**
	Non-volatile	Non-volatile	Volatile				Non-volatile

QP bit

The Quad Page (QP) bit is a volatile Read/Write bit in the Configure Register that allows Quad Page operation. When the QP bit is set to 0 (Default) the page size is 256bytes. When the QP pin is set to 1, the page size is 1024bytes.

This bit controls the page programming buffer address wrap point. Legacy SPI devices generally have used a 256 Byte page programming buffer and defined that if data is loaded into the buffer beyond the 255 Byte locations, the address at which additional bytes are loaded would be wrapped to address zero of the buffer. The ZD25WQ32C provides a 1024Byte page programming buffer that can increase programming performance. For legacy software compatibility, this configuration bit provides the option to continue the wrapping behavior at the 256 Byte boundary or to enable full use of the available 1024Byte buffer by not wrapping the load address at the 256 Byte boundary.

When the QP pin is set to 1, the page erase instruction(81h) will erase the data of the chosen Quad Page to be "1".

DRV1 & DRV0 bit

The DRV1 & DRV0 bits are non-volatile Read/Write bits which are used to determine the output driver strength for the Read operations.

DRV1,DRV0	Drive Strength
0,0	80%
0,1	40%
1,0	100%
1,1(default)	60%

DC bit

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured

Command	DC bit	Numbers of Dummy Cycles	Freq.(MHz)
BBH	0 (default)	4	66
	1	8	86R
EBH	0 (default)	6	66
	1	10	86R

Note:

1. “R” means VCC range=2.3V~3.6V.

3.4 DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset to standby mode automatically during power up. In addition, the control register architecture of the device ensures that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (06H) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# going low to protect the CMP, BP0~BP4 bits and SRP0~1 bits.
- Deep Power-Down Mode: By entering deep power down mode, the flash device is ignores all commands until the Release from Deep Power-Down Mode (B9H) command.

Table-7.1 ZD25WQ32C Protected Area Size (CMP bit=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000H-3FFFFFH	64KB	Upper 1/64
0	0	0	1	0	62 to 63	3E0000H-3FFFFFH	128KB	Upper 1/32
0	0	0	1	1	60 to 63	3C0000H-3FFFFFH	256KB	Upper 1/16
0	0	1	0	0	56 to 63	380000H-3FFFFFH	512KB	Upper 1/8
0	0	1	0	1	48 to 63	300000H-3FFFFFH	1MB	Upper 1/4
0	0	1	1	0	32 to 63	200000H-3FFFFFH	2MB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/64
0	1	0	1	0	0 to 1	000000H-01FFFFH	128KB	Lower 1/32
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/16
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/8
0	1	1	0	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/4
0	1	1	1	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/2
X	X	1	1	1	0 to 63	000000H-3FFFFFH	4MB	ALL
1	0	0	0	1	63	3FF000H-3FFFFFH	4KB	Top Block
1	0	0	1	0	63	3FE000H-3FFFFFH	8KB	Top Block
1	0	0	1	1	63	3FC000H-3FFFFFH	16KB	Top Block
1	0	1	0	X	63	3F8000H-3FFFFFH	32KB	Top Block
1	0	1	1	0	63	3F8000H-3FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table-7.2 ZD25WQ32C Protected Area Size (CMP bit=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H- 3FFFFFH	4MB	ALL
0	0	0	0	1	0 to 62	000000H- 3EFFFFH	4032KB	Lower 63/64
0	0	0	1	0	0 to 61	000000H- 3DFFFFH	3968KB	Lower 31/32
0	0	0	1	1	0 to 59	000000H- 3BFFFFH	3840KB	Lower15/16
0	0	1	0	0	0 to 55	000000H- 37FFFFH	3584KB	Lower 7/8
0	0	1	0	1	0 to 47	000000H- 2FFFFFH	3MB	Lower 3/4
0	0	1	1	0	0 to 31	000000H- 1FFFFFH	2MB	Lower 1/2
0	1	0	0	1	1 to 63	010000H- 3FFFFFH	4032KB	Upper 63/64
0	1	0	1	0	2 to 63	020000H- 3FFFFFH	3968KB	Upper 31/32
0	1	0	1	1	4 to 63	040000H- 3FFFFFH	3840KB	Upper 15/16
0	1	1	0	0	8 to 63	080000H- 3FFFFFH	3584KB	Upper 7/8
0	1	1	0	1	16 to 63	100000H- 3FFFFFH	3MB	Upper 3/4
0	1	1	1	0	32 to 63	200000H- 3FFFFFH	2MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 63	000000H-3FEFFFH	4092KB	L-1023/1024
1	0	0	1	0	0 to 63	000000H- 3FDFFFH	4088KB	L-511/512
1	0	0	1	1	0 to 63	000000H-3FBFFFH	4080KB	L-255/256
1	0	1	0	X	0 to 63	000000H-3F7FFFH	4064KB	L- 127/128
1	0	1	1	0	0 to 63	000000H-3F7FFFH	4064KB	L- 127/128
1	1	0	0	1	0 to 63	001000H-3FFFFFH	4092KB	U- 1023/1024
1	1	0	1	0	0 to 63	002000H-3FFFFFH	4088KB	U- 511/512
1	1	0	1	1	0 to 63	004000H-3FFFFFH	4080KB	U- 255/256
1	1	1	0	X	0 to 63	008000H-3FFFFFH	4064KB	U- 127/128
1	1	1	1	0	0 to 63	008000H-3FFFFFH	4064KB	U- 127/128

Notes:

1. X=don’t care
2. If any erase or program command specifies a memory that contains protected data portion, this command will be ignored.

4. COMMAND DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted into the device starting with the most significant bit on SI. Each bit is latched on the rising edge of SCLK.

The commands supported by ZD25WQ32C are listed inTable-8. Every command sequence starts with a one-byte command code. Depending on the command, it might be followed by address or data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the commands of Read, Fast Read, Read Status Register, Release from Deep Power- Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read commands can be completed after any bit of the data-out sequence is shifted out, and then CS# must be driven high to return to deselected status.

For the Page Program , Sector Erase , Half Block Erase , Block Erase , Chip Erase , Write Status Register , Write Enable , Write Disable or Deep Power-Down commands, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That means CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if CS# is driven high at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table-8. Commands (Standard/Dual/Quad SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Volatitle SR Write Enable	50H								
Read Status Register-1	05H	(S7-S0)	(cont.)						
Read Status Register-2	35H	(S15-S8)	(cont.)						
Read Configure Register	45/15H	(S7-S0)	(cont.)						
Write Status Register-1	01H	S7-S0							
Write Status Register-1&2	01H	S7-S0	S15-S8						
Write Status Register-2	31H	S15-S8							
Write Configure Register	11H	S7-S0							
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Read Word Quad I/O	E7H	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)	
Read Octal Word Quad I/O	E3H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual I/O Fast Read	BBH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Active Status Interrupt	25H								
Quad I/O Fast Read	EBH	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	(cont.)

Commands (Standard/Dual/Quad SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte8	Byte 9	Byte 10
Set Burst with Wrap	77H	dummy	dummy	dummy	W7-W0					
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Dual-IN Page Program	A2H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Page Erase	81H	A23-A16	A15-A8	A7-A0						
Sector Erase	20H	A23-A16	A15-A8	A7-A0						
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0						
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0						
Chip Erase	C7/60H									
Read Manufacturer/Device ID	90H	dummy	dummy	A7-A0	(MID7-MID0)	(ID7-ID0)	(cont.)			
Dual I/O Read Manufacturer/Device ID	92H	dummy	dummy	A7-A0	dummy	(MID7-MID0)	(ID7-ID0)	(cont.)		
Quad I/O Read Manufacturer/Device ID	94H	dummy	dummy	A7-A0	dummy	dummy	dummy	(MID7-MID0)	(ID7-ID0)	(cont.)
Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)					
Read Unique ID	4BH	dummy	dummy	dummy	dummy	(UID7-UID0)	(cont.)			
Erase Security Registers	44H	A23-A16	A15-A8	A7-A0						
Program Security Registers	42H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Read Security Registers	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)			
Enable Reset	66H									
Reset	99H									
Program/Erase Suspend	75H/B0H									
Program/Erase Resume	7AH/30H									
Deep Power-Down	B9H									
Release From Deep Power-Down	ABH									
Release From Deep Power-Down and Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)				
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)			

Notes:

1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)

2. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1

3. Quad Output Data
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3,…..)

4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0
   IO1 = A21, A17, A13, A9, A5, A1
   IO2 = A22, A18, A14, A10, A6, A2
   IO3 = A23, A19, A15, A11, A7, A3

5. Fast Read Quad I/O Dummy Bits and Data
   IO0 = (x, x, x, x, D4, D0,…)
   IO1 = (x, x, x, x, D5, D1,…)
   IO2 = (x, x, x, x, D6, D2,…)
   IO3 = (x, x, x, x, D7, D3,…)

6. Word Read Quad I/O Data
   IO0 = (x, x, D4, D0,…)
   IO1 = (x, x, D5, D1,…)
   IO2 = (x, x, D6, D2,…)
   IO3 = (x, x, D7, D3,…)

7. Security Registers Address:
   Security Register1: A23-A16=00H, A15-A12=1H, A11-A10 = 00b, A9-A0= Byte Address;
   Security Register2: A23-A16=00H, A15-A12=2H, A11-A10 = 00b, A9-A0= Byte Address;
   Security Register3: A23-A16=00H, A15-A12=3H, A11-A10 = 00b, A9-A0= Byte Address;

8. Dummy bits and Wrap Bits
   IO0 = (x, x, x, x, x, x, W4, x)
   IO1 = (x, x, x, x, x, x, W5, x)
   IO2 = (x, x, x, x, x, x, W6, x)
   IO3 = (x, x, x, x, x, x, x, x)

9. Address, Dummy bits, Manufacture ID and Device ID

IO0 = (A20, A16, A12, A8, A4, A0, x, x, x, x, x, x, MID4, MID0, DID4, DID0, …)

IO1 = (A21, A17, A13, A9, A5, A1, x, x, x, x, x, x, MID5, MID1, DID5, DID1, …)

IO2 = (A22, A18, A14, A10, A6, A2, x, x, x, x, x, x, MID6, MID2, DID6, DID2, …)

IO3 = (A23, A19, A15, A11, A7, A3, x, x, x, x, x, x, MID7, MID3, DID7, DID3, …)

10. A0 must be 0 for Word Read 4xI/O. A0-A3 must be 0 for Octal Word Read.

Tables of ID Definition:

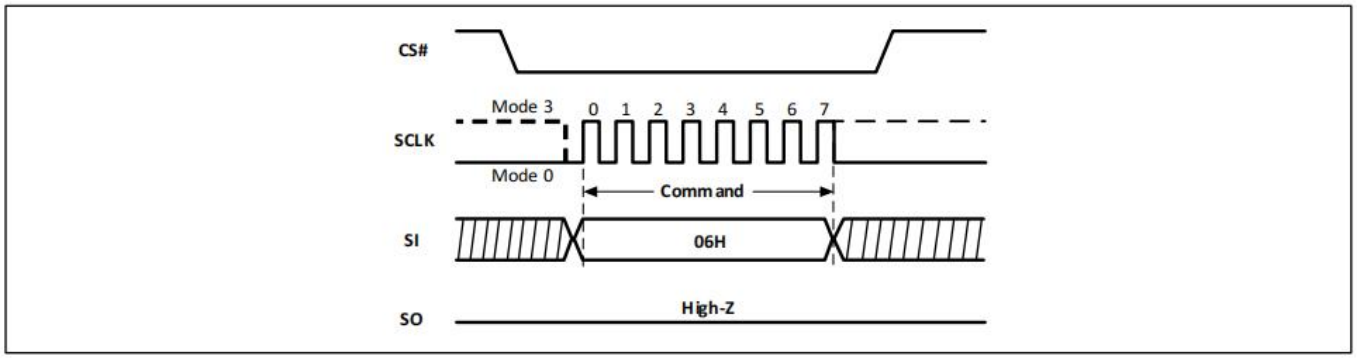
Table-9 ZD25WQ32C

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	BA	60	16
90H/92H/94H	BA		15
ABH			15

4.1 Write Enable (WREN) (06H)

The Write Enable (06H) command sets the Write Enable Latch (WEL) bit. The WEL bit must be set prior to every Page Program, Page Erase, Sector Erase, Half Block Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Register command. The WREN command is entered by driving Chip Select (CS#) Low, sending the command code, and then driving CS# High.

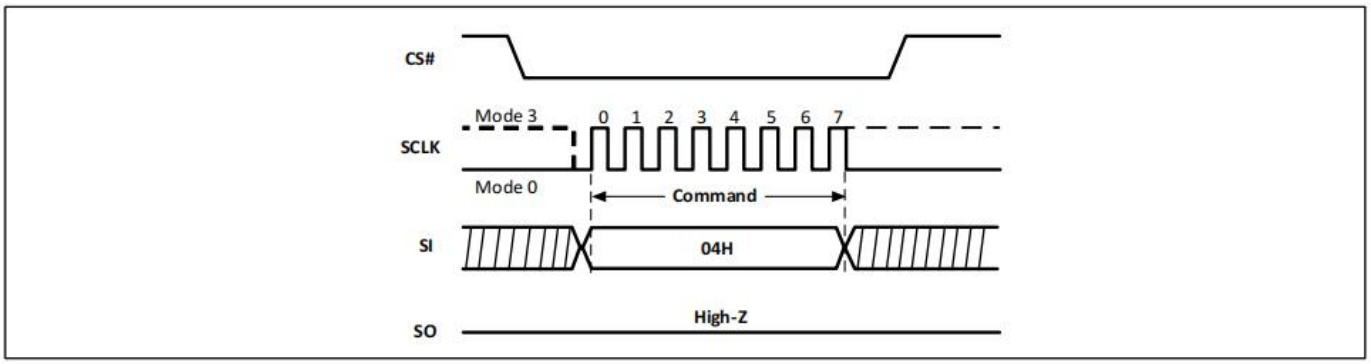
Figure-3. Write Enable Sequence Diagram



4.2 Write Disable (WRDI) (04H)

The Write Disable (04H) command resets the Write Enable Latch (WEL) bit in the Status Register to 0. The WRDI command is entered by driving Chip Select (CS#) low, shifting the command code “04h” into the SI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Page Erase, Sector Erase, Half Block Erase, Block Erase, Chip Erase, Erase/Program Security Register and Reset commands.

Figure-4. Write Disable Sequence Diagram

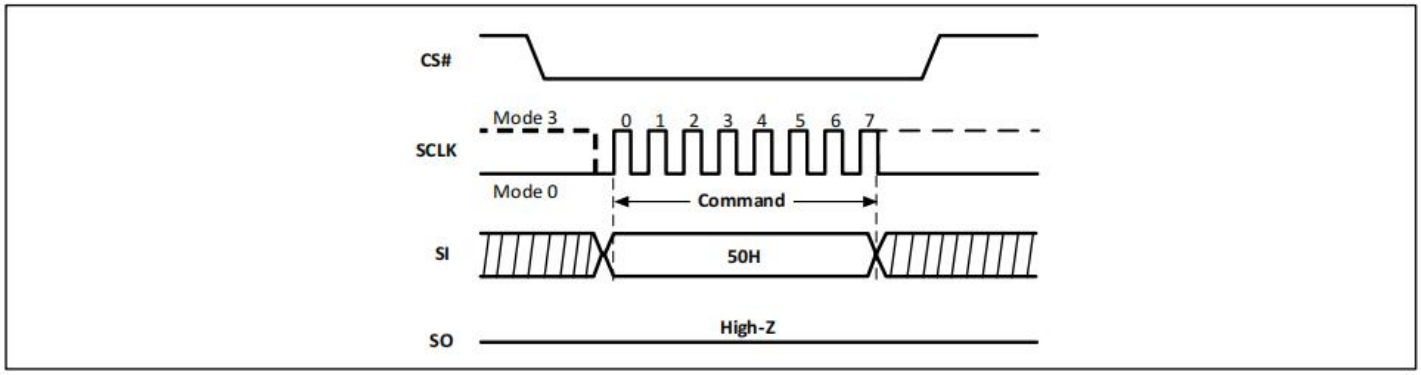


4.3 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This provides more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50H) command must be issued and immediately followed by the Write Status Register (01H/11H/31H) command. Write Enable for Volatile Status Register command (Figure-5) will not set the Write Enable Latch (WEL) bit, it is only valid for the next Write Status Register command, to change the volatile Status Register bit values.

Figure-5. Write Enable for Volatile Status Register Sequence Diagram

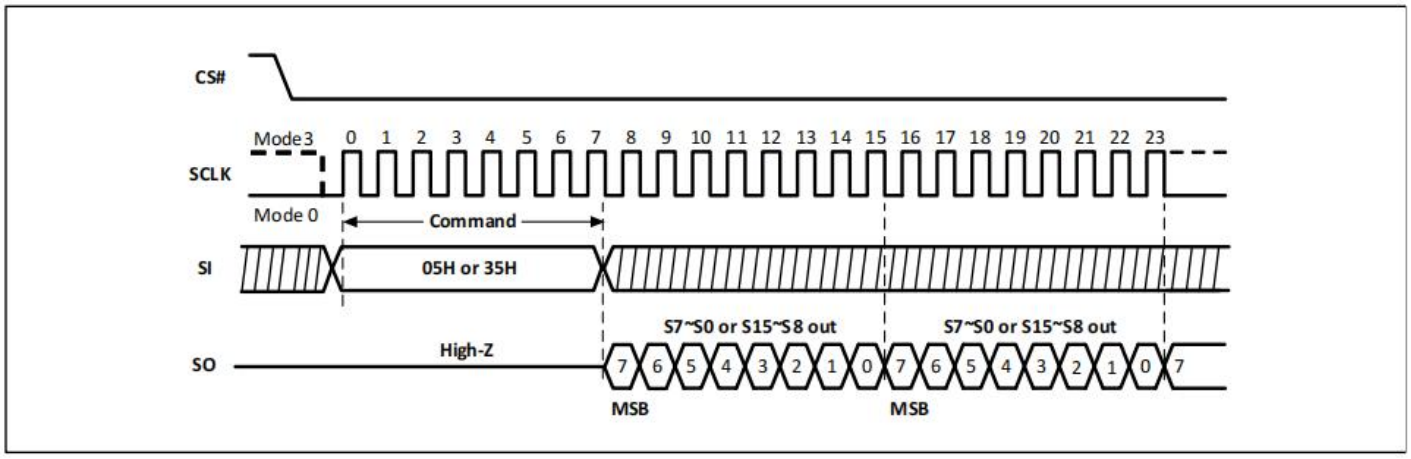


4.4 Read Status Register (RDSR) (05H, 35H)

The Read Status Register (05H or 35H) command allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. And for command code “35H”, the SO will output Status Register bits S15~S8.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Figure-6. Read Status Register Sequence Diagram



4.5 Active Status Interrupt (ASI) (25H)

The Active Status Interrupt (25h) command provides an alternative method to read the Write In Progress (WIP) bit. The SO pin outputs the WIP bit continuously with the ASI command. The SO pin can be connected to an interrupt line of the host controller, and the host controller remains in sleep mode until the SO pin indicates that the device is ready for the next command.

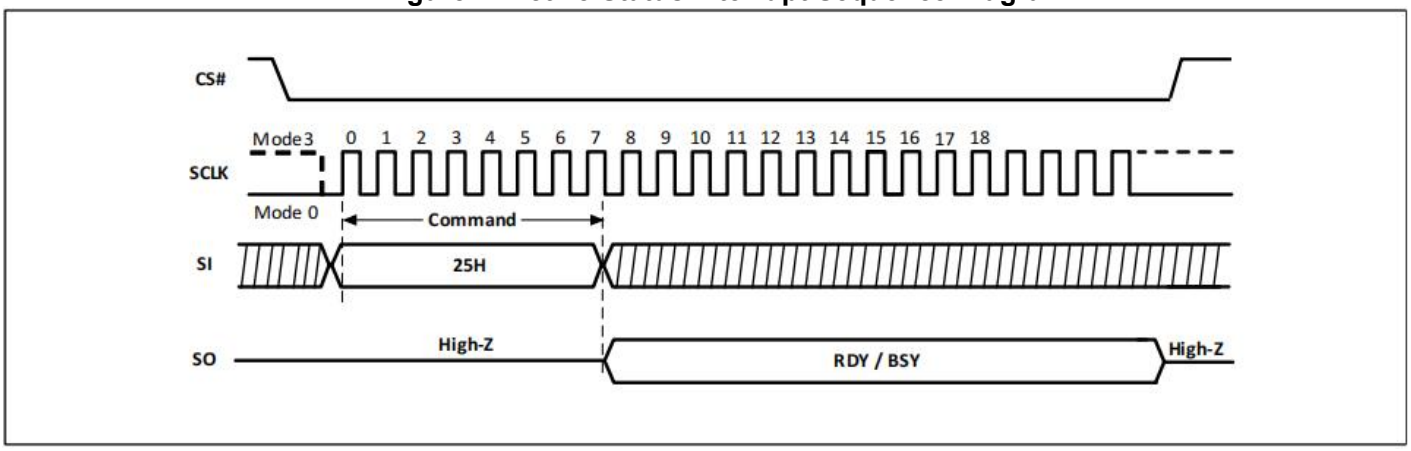
The WIP bit can be read at any time, including while an internally self-timed program or erase operation is in progress. To enable the ASI command, the CS# pin must first be asserted and the opcode of 25h must be clocked into the device.

The value of WIP is then output on the SO pin and is continuously updated by the device for as long as the CS# pin remains asserted. Additional clocks on the SCLK pin are not required. If the WIP bit changes from 1 to 0 while the CS# pin is asserted, the SO pin will change from 1 to 0 when the program/erase operation is completed. (The WIP bit cannot change from 0 to 1 during an operation, so if the SO pin already is 0, it will not change.)

Deserting the CS# pin will terminate the ASI operation and put the SO pin into a high-impedance state. The CS# pin can be deserted at any time and does not require that a full byte of data be read.

The sequence of issuing ASI command is: CS# goes low -> send Active Status Interrupt (25H) command code -> Write In Progress (WIP) data out on SO.

Figure-7. Active Status Interrupt Sequence Diagram



4.6 Write Status Register (WRSR) (01H or 31H)

WRSR can write 8bits or 16bits data. The Write Status Register (01H for one byte or two bytes, 31H for one byte only) command allows new values to be written to the Status Register. Command 01H is used to write S7~S0 (one byte) S15~S8 will keep original value or S15~S0(two bytes). Command 31H is used to write S15~S8. Before the command can be accepted, a Write Enable (06H) command must previously have been executed. After the Write Enable command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The WRSR command is entered by driving Chip Select (CS#) Low, followed by the command code and the data byte on Data Input (SI).

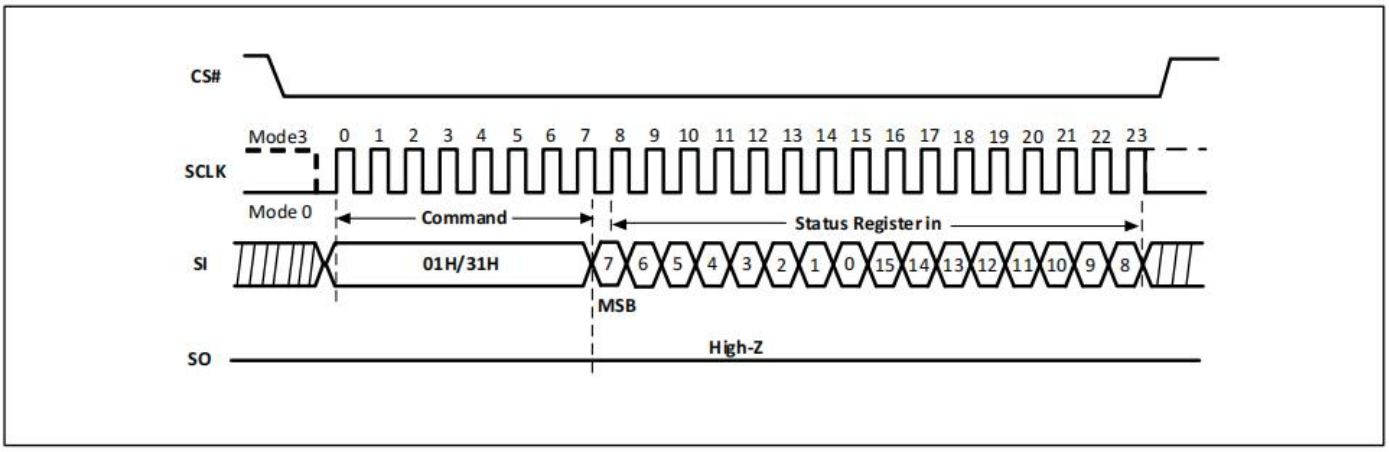
The WRSR command has no effect on S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the sixteenth bit or eighth bit of the data byte has been latched in. If not, the WRSR command is not executed. As soon as CS# is driven High, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Write Status Register cycle and is 0 when it is completed. When the cycle is completed, the WEL bit is reset.

The WRSR command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1,

BP0) bits. The WRSR command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and WP# signal allow the device to be put in the Hardware Protection Mode. The WRSR command is not executed once the Hardware Protection Mode is entered.

CS# must go high exactly at the 8bit or 16bit data boundary; otherwise the command will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as CS# goes high. The WIP bit still can be checked during the Write Status Register cycle is in progress. The WIP is set to 1 during tW and is reset to 0 along with the WEL bit when Write Status Register Cycle is completed.

Figure-8. Write Status Register Sequence Diagram



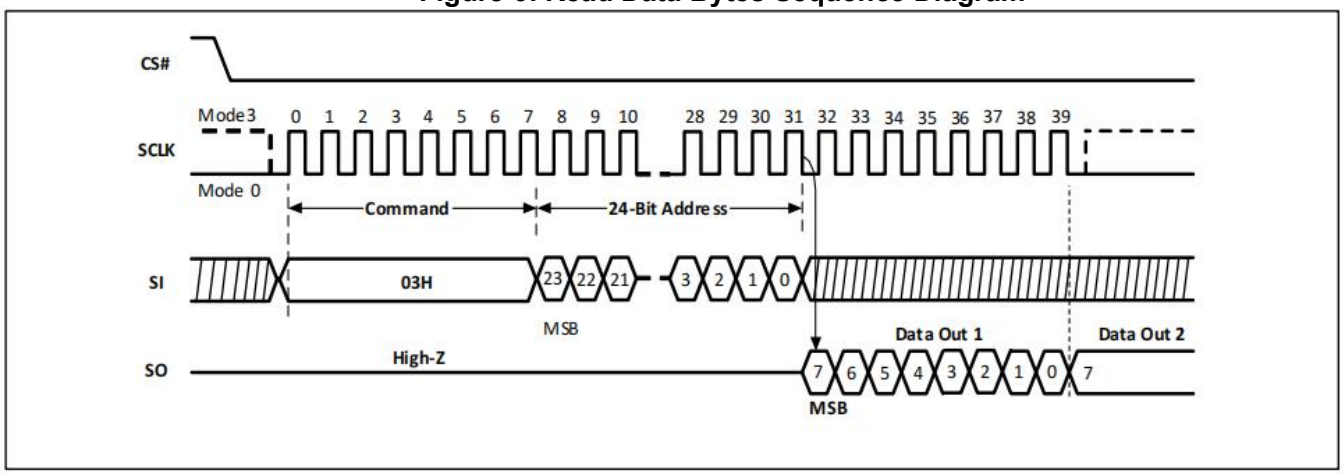
4.7 Read Data Bytes (READ) (03H)

The device is first selected by driving Chip Select (CS#) Low. The command code for the Read Data Bytes (03H) command is followed by a 3-byte address (A23-A0), with each bit latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at that address, is shifted out on Data Output (SO), with each bit shifted out at a maximum frequency fR on the falling edge of SCLK.

The command sequence is shown in Figure-9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single READ command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The READ command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any READ command to the memory array, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-9. Read Data Bytes Sequence Diagram



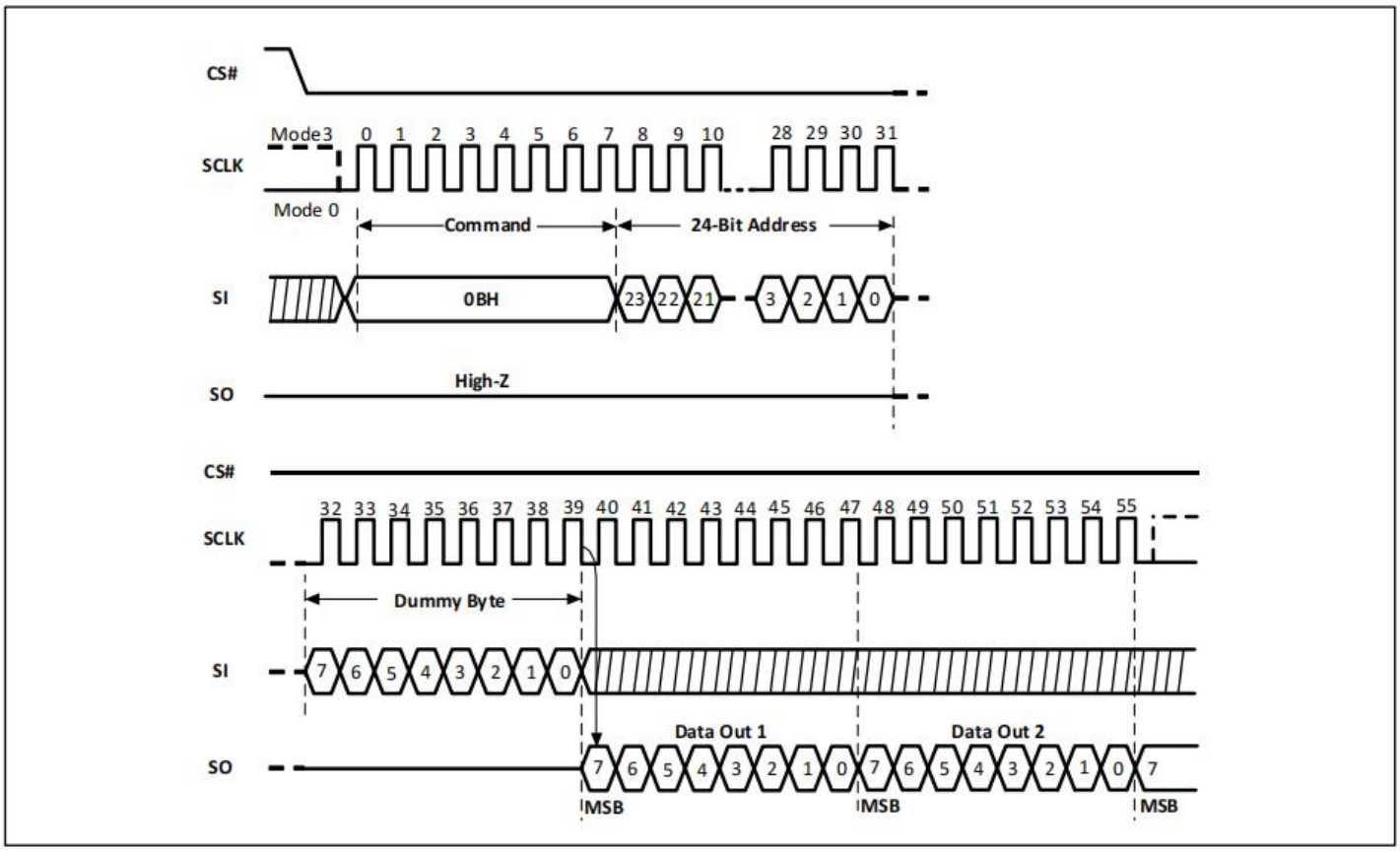
4.8 Read Data Bytes at Higher Speed (FAST_READ) (0BH)

The device is first selected by driving Chip Select (CS#) Low. The command code for the Read Data Bytes at Higher Speed (0BH) command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at that address, is shifted out on Data Output (SO), with each bit shifted out at a maximum frequency fC on the falling edge of SCLK.

The command sequence is shown in Figure-10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single FAST_READ command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The FAST_READ command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any FAST_READ command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-10. Read Data Bytes at Higher Speed Sequence Diagram

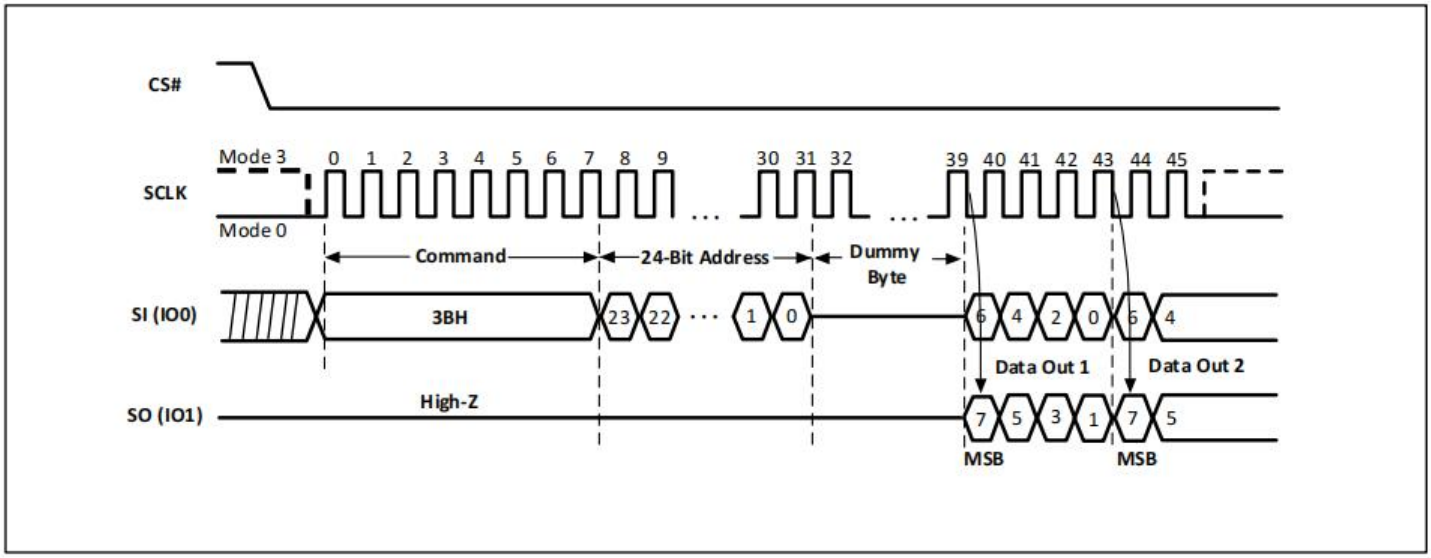


4.9 Dual Output Fast Read (DREAD) (3BH)

The Dual Output Fast Read (3BH) is similar to the standard Fast Read (0BH) command except that data is output on two pins, SI (IO0) and SO (IO1), instead of just SO. This allows data to be transferred from the ZD25WQxx at twice the rate of standard SPI devices. The DREAD command is ideal for quickly downloading code from the flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Like the Fast Read command, the DREAD command can operate at the highest possible frequency of fT. This is accomplished by adding eight “dummy clocks after the 24-bit address as shown in Figure-11. The dummy clocks allow the device’s internal circuits the time required for setting up the initial address. The input data during the dummy clock is “don’t care”. However, the SI pin should be in a high-impedance state prior to the falling edge of SLCK for the first data out.

Figure-11. Dual Output Fast Read Sequence Diagram

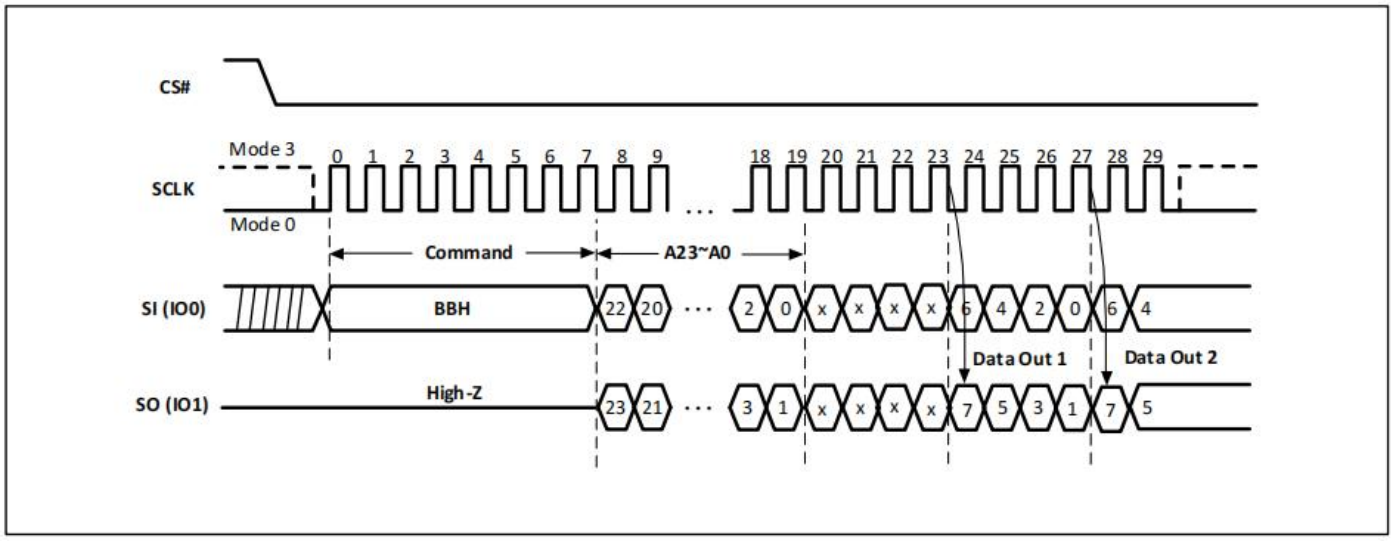


4.10 Dual I/O Fast Read (2READ) (BBH)

The Dual I/O Fast Read (BBH) command allows for improved random access while maintaining two IO pins, SI (IO0) and SO (IO1). It is similar to the Dual Output Fast Read (3BH) command but with the ability to input the address bits (A23-0) two bits per clock. This reduced command overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The 2READ command enables double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and two bits of data (interleave 2 I/O pins) are shifted out on the falling edge of SCLK at a maximum frequency fT. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out with a single 2READ command. The address counter rolls over to 0 when the highest address has been reached. The 2READ command is shown in Figure-12.

Figure-12. Dual I/O Fast Read Sequence Diagram

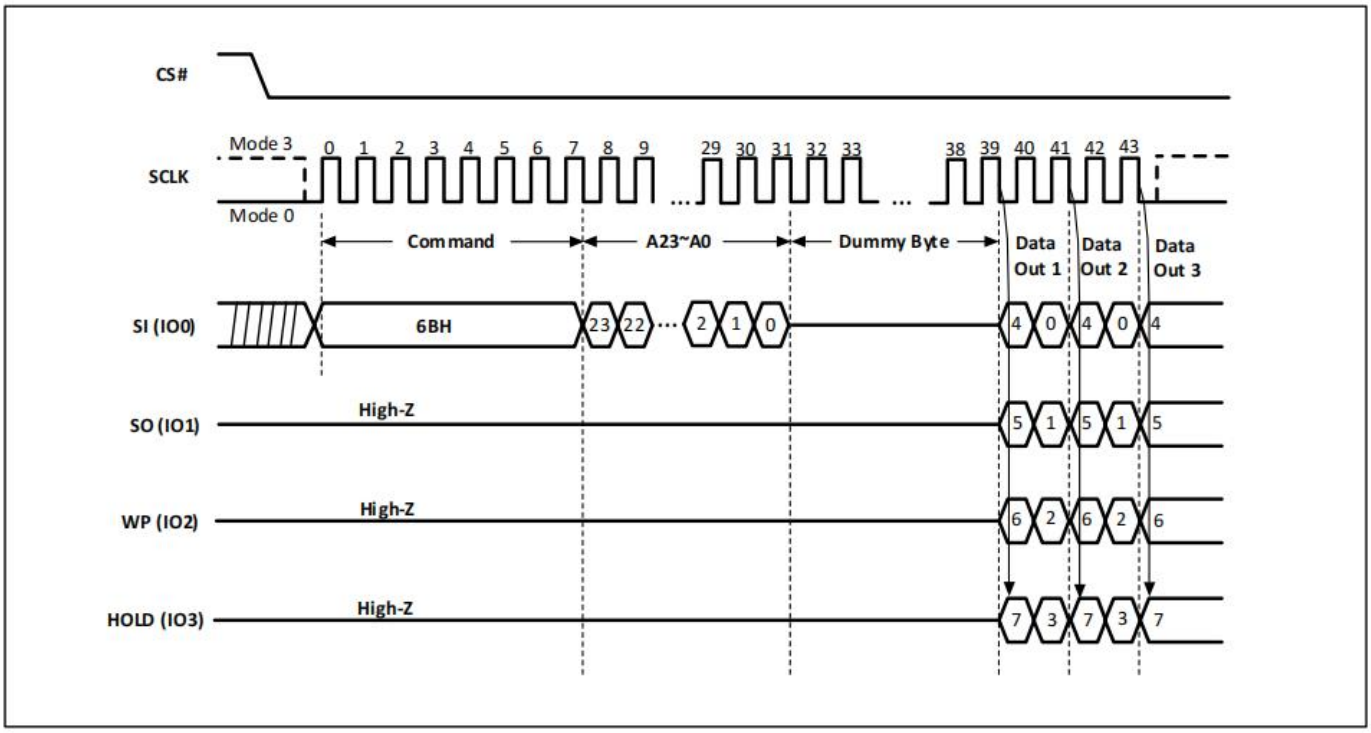


4.11 Quad Output Fast Read (QREAD) (6BH)

The Quad Output Fast Read (6BH) command is similar to the Dual Output Fast Read (3BH) command except that data is output on four pins, IO0, IO1, IO2, and IO3. A Quad Enable (QE) of Status Register-2 must be executed before the device will accept the QREAD Command. (The QE bit must equal “1”). The QREAD Command allows data to be transferred at four times the rate of standard SPI devices.

The QREAD command can operate at a higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure-13. The dummy clocks allow the device's internal circuits the time required for setting up the initial address. The input data during the dummy clocks is “don’t care.” However, the IO pins should be in a high-impedance state prior to the falling edge of SCLK for the first data out.

Figure-13. Quad Output Fast Read Sequence Diagram



4.12 Quad I/O Fast Read (4READ) (EBH)

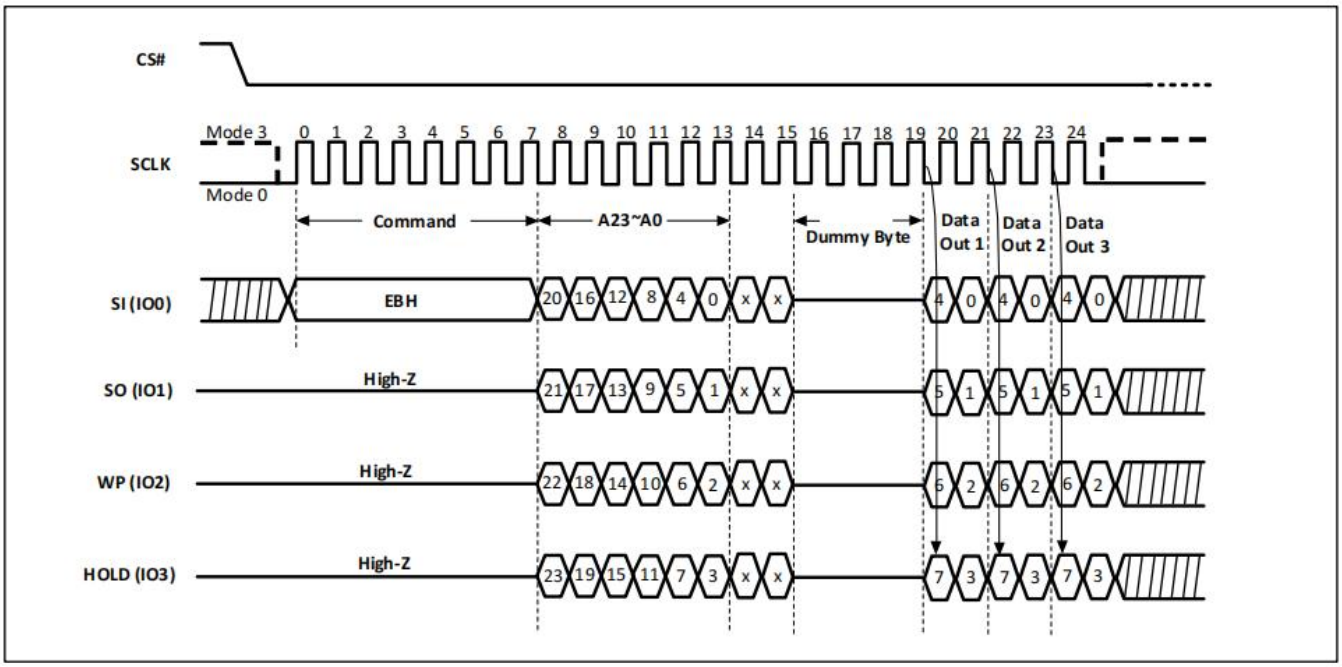
The Quad I/O Fast Read (EBH) command is similar to the Dual I/O Fast Read (BBH) command except that address and data bits are input and output through four pins, SI (IO0), SO (IO1), WP (IO2) and HOLD (IO3). Six dummy clocks are required prior to the data output. A Quad Enable (QE) of Status Register-2 must be executed before the device will accept the 4READ Command. (The QE bit must equal “1”). The Quad I/O dramatically reduces command overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The 4READ command enables quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data four bits of data (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out with a single 4READ command. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ command, the following address / dummy / data out will transfer 4-bits per clock cycle instead of the previous 1-bit.

The sequence of issuing 4READ command is: CS# goes low -> send Quad I/O Fast Read (EBH) command -> 24-bit address interleave on IO3, IO2, IO1 and IO0 -> 2+4 dummy cycles -> data out interleave on IO3, IO2, IO1 and IO0 -> end 4READ operation by driving CS# high at any time during data out, as shown in Figure-14.

Another sequence of issuing 4READ command especially useful in random access is: CS# goes low -> send Quad I/O Fast Read (EBH) command -> 24-bit address interleave on IO3, IO2, IO1 and IO0 -> 6 dummy cycles -> data out until CS# goes high -> CS# goes low (reduce 4READ command) -> 24-bit random access address.

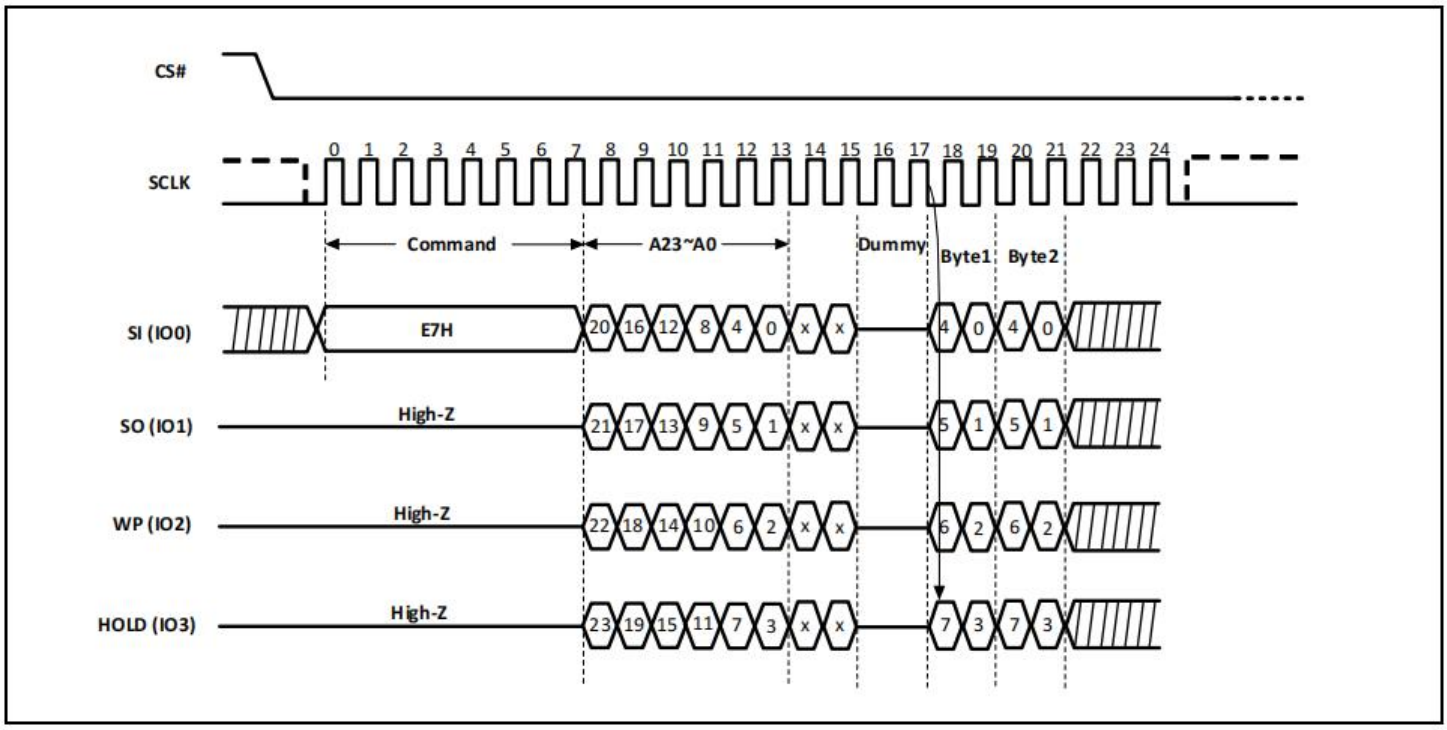
Figure-14. Quad I/O Fast Read Sequence Diagram



4.13 Quad I/O Word Read (E7H)

The Quad I/O Word Read command is similar to the Quad I/O Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word read command.

Figure-15. Quad I/O Word Read Sequence



Quad I/O Word Read with "8/16/32/64-Byte Wrap Around"

The Quad I/O Word Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to E7H. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following E7H commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

4.14 Quad I/O Octal Word Read (E3H)

The Quad IO Octal Word Read (E3h) instruction is similar to the Quad IO Read (EBH) instruction except that the lower four Address bits (A0, A1, A2, A3) must equal 0. As a result, the dummy clocks are not required, which further reduces the instruction overhead allowing even faster random access for code execution (XIP). The Quad Enable bit (QE) of Status Register-2 must be set to enable the Octal Word Read Quad I/O Instruction.

4.15 Set Burst with Wrap (77H)

The Set Burst with Wrap (77h) command is used in conjunction with Quad I/O Fast Read (EBH/E7H) command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

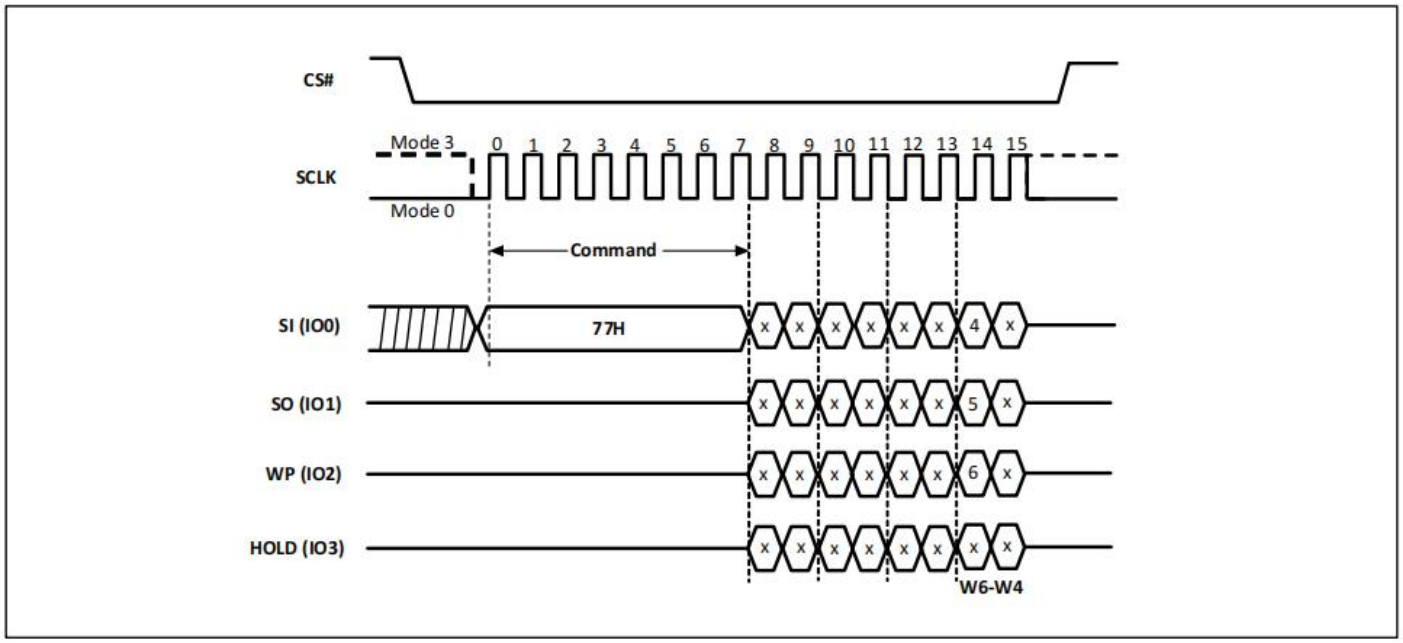
The Set Burst with Wrap command sequence: CS# goes low -> Send Set Burst with Wrap (77h) command -> Send 24 dummy bits-> Send 8 bits "Wrap bits" -> CS# goes high.

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following Quad I/O Fast Read commands will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Table-10. Burst Length and Wrap

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0,0	Yes	8-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

Figure-16. Set Burst with Wrap Sequence Diagram



4.16 Page Erase (PE) (81H)

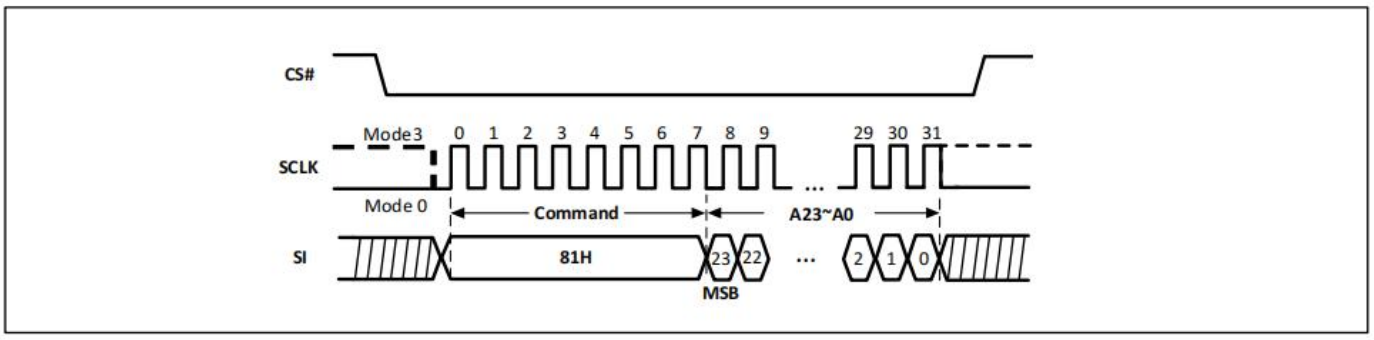
The Page Erase (81H) command sets all bits to 1 (FFH) inside the chosen page. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The PE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the page is a valid address for the PE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-17. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Page Erase cycle (with duration tPE) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Page Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A PE command may be applied only to a page which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-17. Page Erase Sequence Diagram



4.17 Sector Erase (SE) (20H)

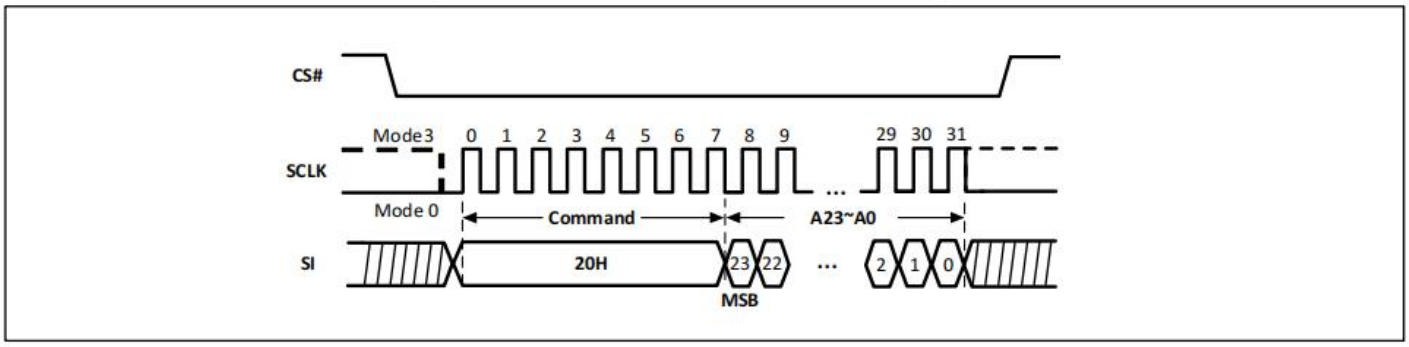
The Sector Erase (20H) command sets all bits to 1 (FFH) inside the chosen sector. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The SE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the sector is a valid address for the SE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-18. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Sector Erase cycle (with duration tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Sector Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A SE command may be applied only to a sector which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-18. Sector Erase Sequence Diagram



The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP4, BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector

4.18 Half Block Erase (HBE) (52H)

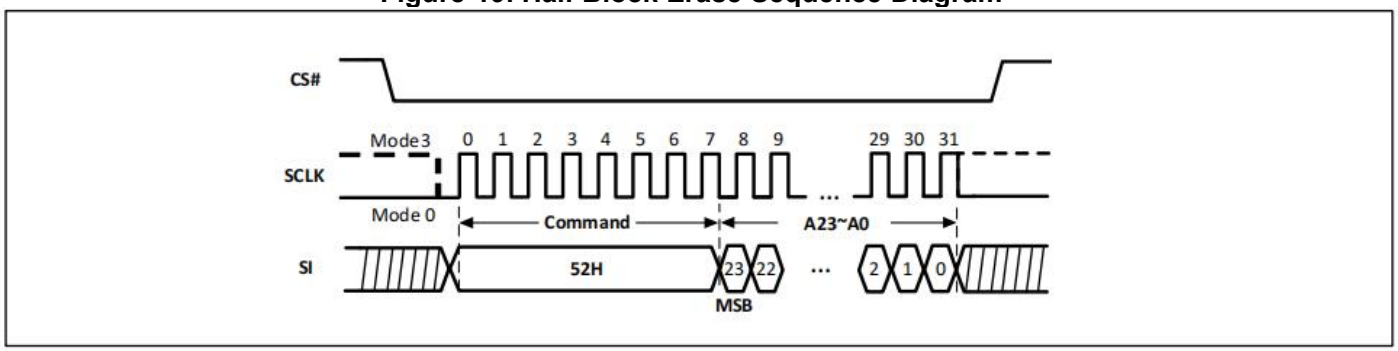
The Half Block Erase (52H) command sets all bits to 1 (FFH) inside the chosen block. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The HBE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the block is a valid address for the HBE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-19. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Half Block Erase cycle (with duration tBE1) is initiated. While the Half Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A HBE command may be applied only to a half block which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-19. Half Block Erase Sequence Diagram



4.19 Block Erase (BE) (D8H)

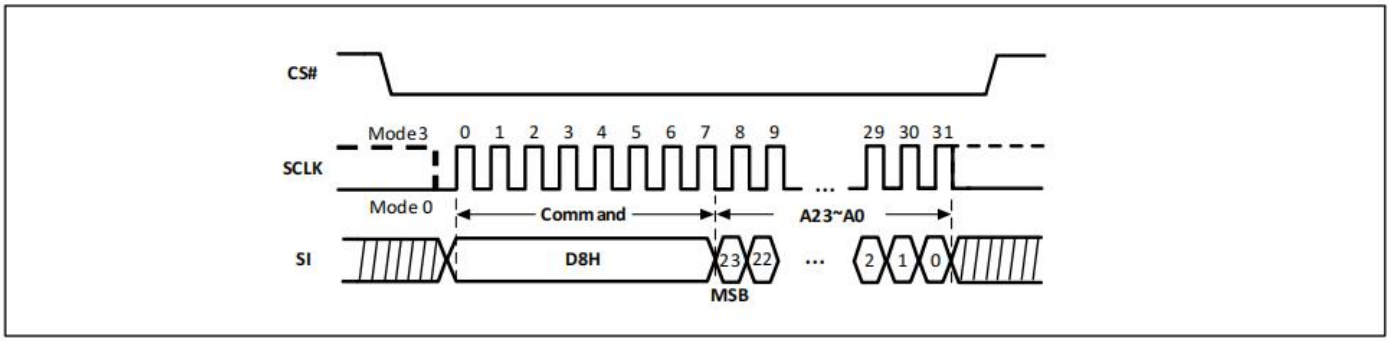
The Block Erase (D8H) command sets all bits to 1 (FFH) inside the chosen block. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable 06H command has been decoded, the device sets the Write Enable Latch (WEL).

The BE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the block is a valid address for the BE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-20. CS# must be driven High after the least significant bit of the third address byte is latched in, otherwise the BE command is not executed. As soon as CS# is driven High, the self-timed Block Erase cycle (whose duration is tBE2) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A BE command may be applied only to a block which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-20. Block Erase Sequence Diagram



4.20 Chip Erase (CE) (60H or C7H)

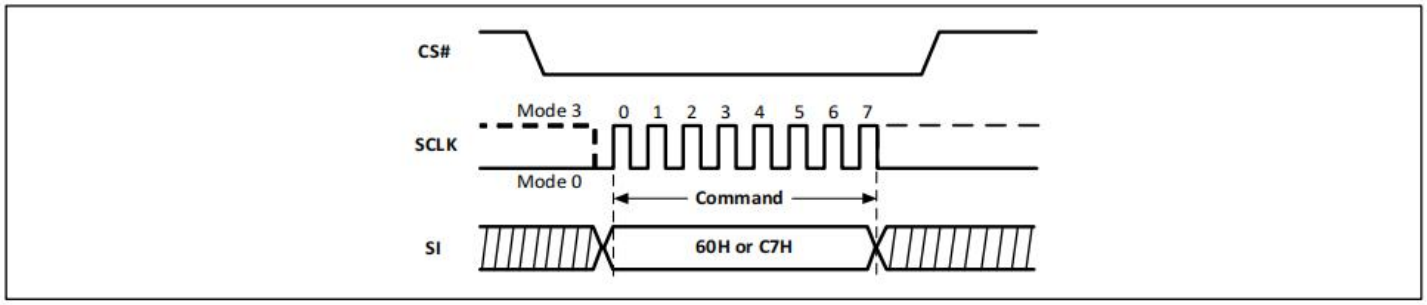
The Chip Erase (60H or C7H) command sets all bits to 1 (FFH). Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The CE command is entered by driving Chip Select (CS#) Low, followed by the command code on Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-21. CS# must be driven High after the eighth bit of the command code is latched in, otherwise the CE command is not executed. As soon as CS# is driven High, the self-timed Chip Erase cycle (with duration tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Chip Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

The CE command is executed only if all Block Protect (BP4, BP3, BP2, BP1, BP0) bits are 0. The CE command is ignored if one, or more blocks are protected.

Figure-21. Chip Erase Sequence Diagram



4.21 Page Program (PP) (02H)

The Page Program (02H) command allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The PP command is entered by driving Chip Select (CS#) Low, followed by the command code, three address bytes and at least one data byte on Data Input (SI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the starting address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven Low for the entire duration of the sequence.

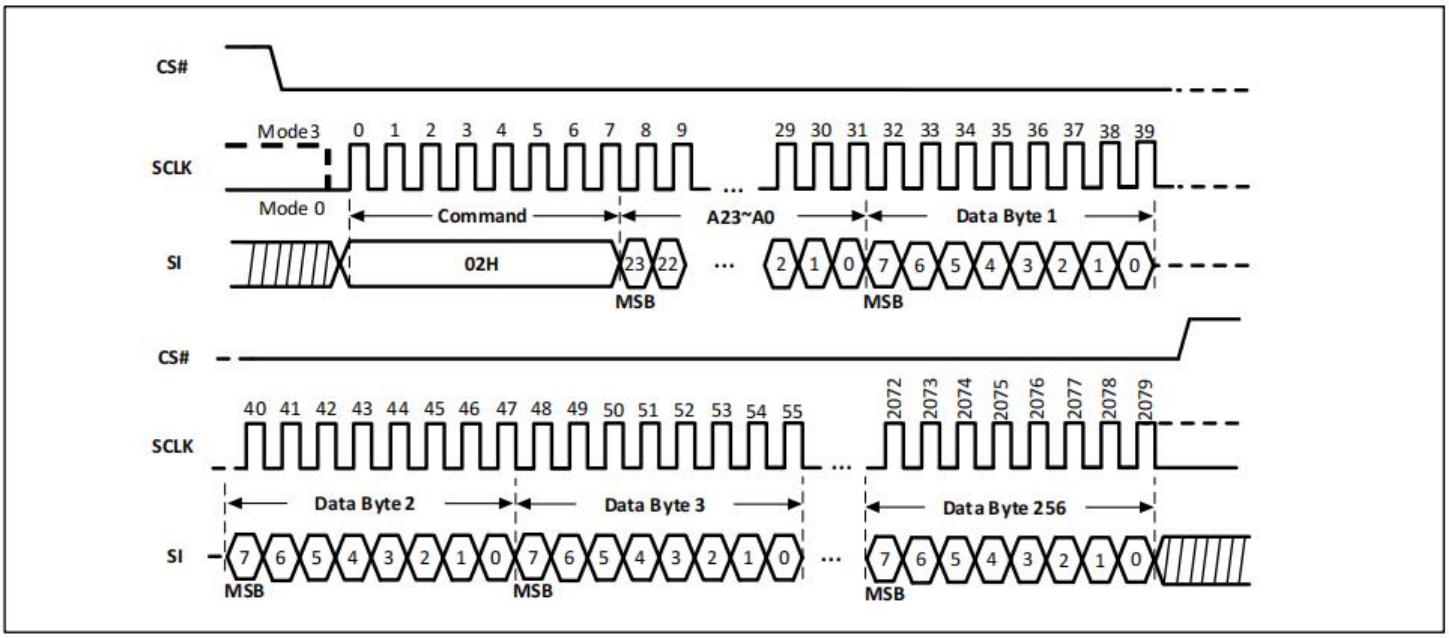
The command sequence is shown in Figure-22. If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

CS# must be driven High after the eighth bit of the last data byte has been latched in, otherwise the PP command is not executed.

As soon as CS# is driven High, the self-timed Page Program cycle (with duration tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the WIP bit. The WIP bit is 1 during the self-timed Page Program cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A PP command may be applied only to a page which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-22. Page Program Sequence Diagram



4.22 Dual Input Page Program (DPP) (A2H)

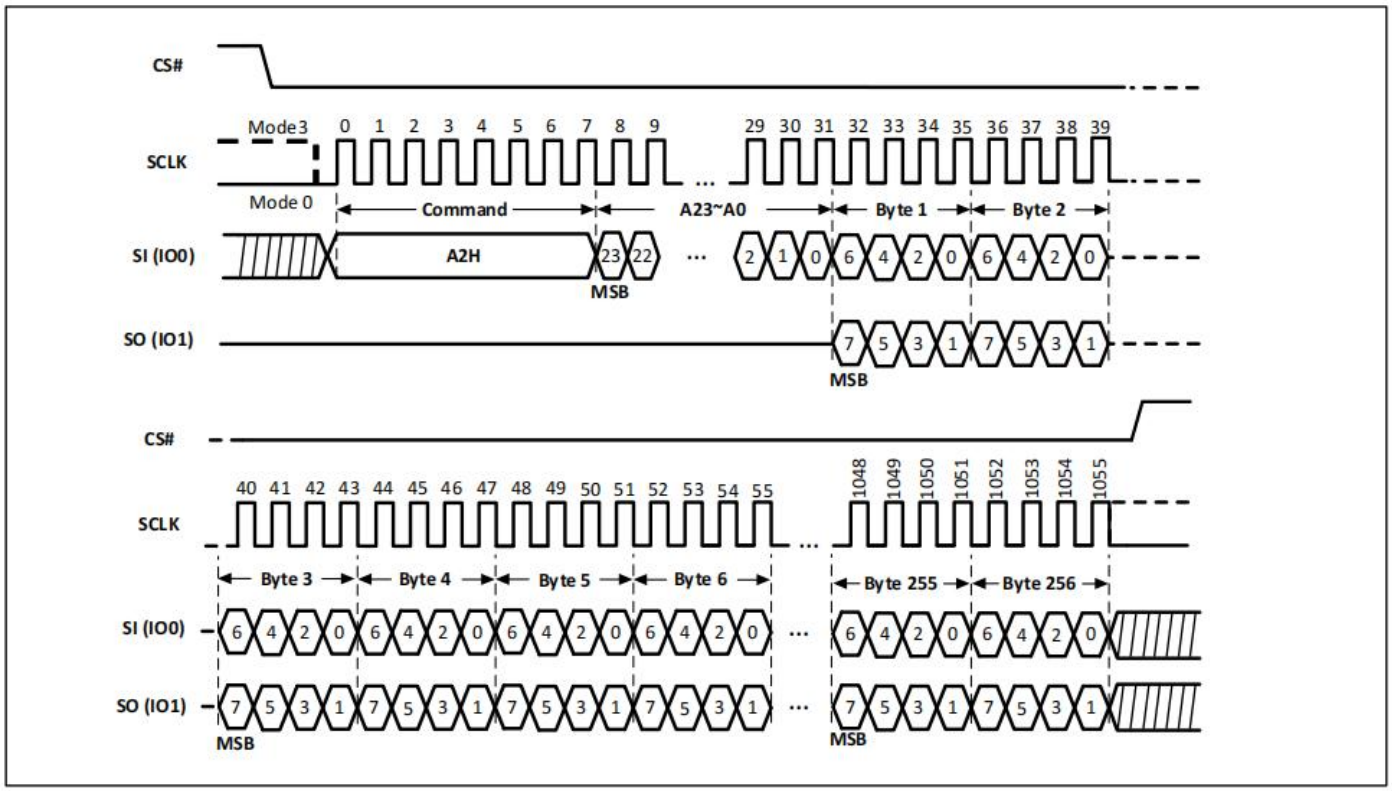
The Dual Input Page Program (A2H) command is similar to the standard Page Program command and can be used to program anywhere from a single byte of data up to 256 bytes of data into previously erased memory locations. The DPP command allows two bits of data to be clocked into the device on every clock cycle rather than just one.

A Write Enable (06H) command must be executed to set the Write Enable Latch (WEL) bit before sending the DPP command. The Dual Input Page Programming takes two pins: IO0, IO1 as data input, which can improve programmer as well as in-system application performance. The other function descriptions are as same as the standard page program.

The sequence of issuing DPP command is: CS# goes low -> send Dual Input Page Program (A2H) command code -> 3-byte address on SI -> at least 1-byte on data on IO[1:0] -> CS# goes high.

A DPP command may be applied only to a page which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-23. Dual Input Page Program Diagram



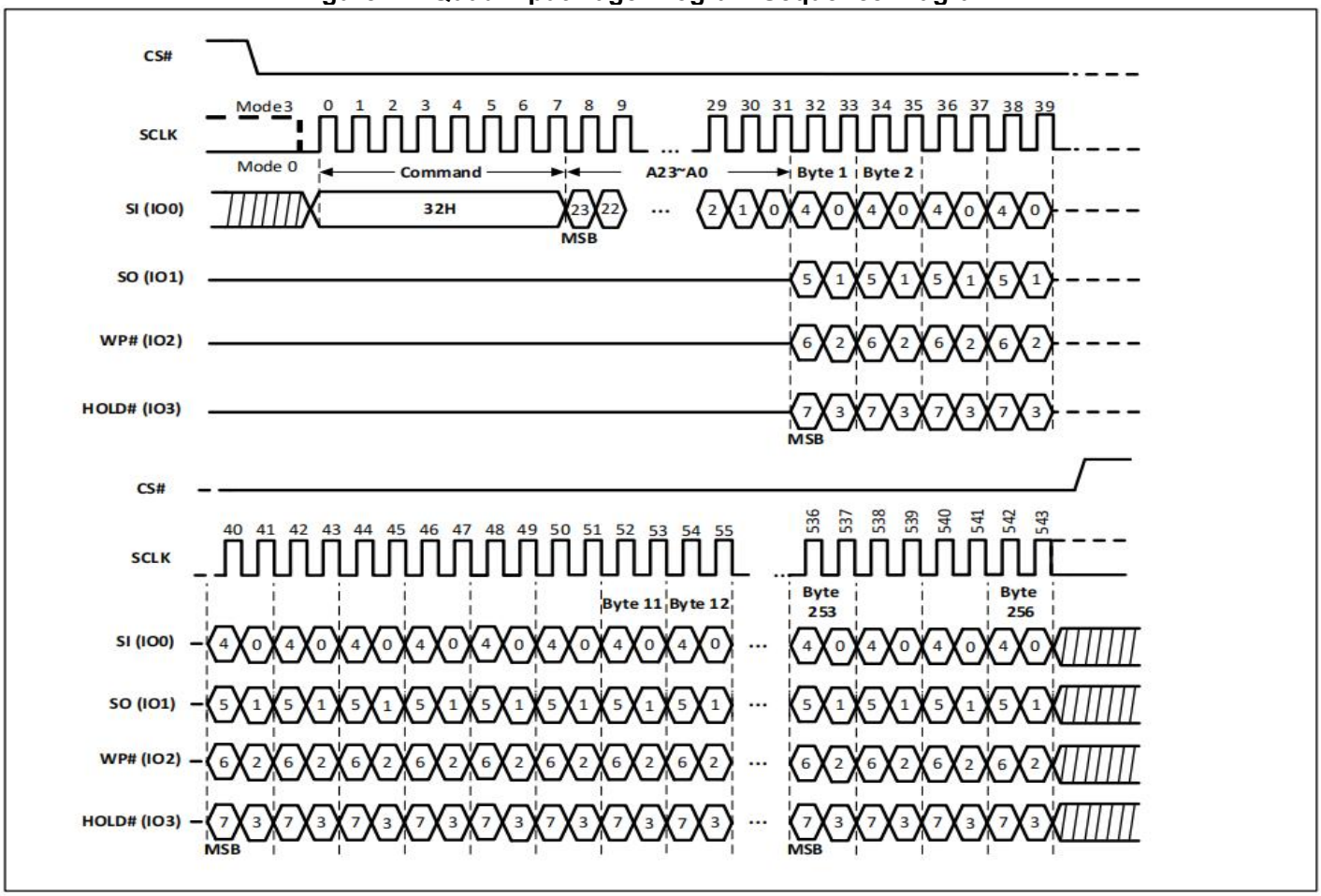
4.23 Quad Input Page Program (QPP) (32H)

The Quad Input Page Program (32H) command is for programming the memory to be "0". A Write Enable command must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit to "1" before sending the QPP command. The Quad Input Page Programming uses four pins: IO0, IO1, IO2, and IO3 as data input, which can improve programmer as well as in-system application performance. The QPP operation supports frequencies as fast as fQPP. The other function descriptions are as same as standard page program.

The sequence of issuing QPP command is: CS# goes low -> send Quad Input Page Program (32H) command code -> 3-byte address on IO0 -> at least 1-byte on data on IO[3:0] -> CS# goes high.

A QPP command may be applied only to a page which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-24. Quad Input Page Program Sequence Diagram



4.24 Erase Security Register (ERSCUR) (44H)

There are three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register (44H) command is like the Sector Erase (20H) command. A Write Enable command must be executed before the device will accept the ERSCUR Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “44H” followed by a 24-bit address (A23-A0) to erase one of the security registers.

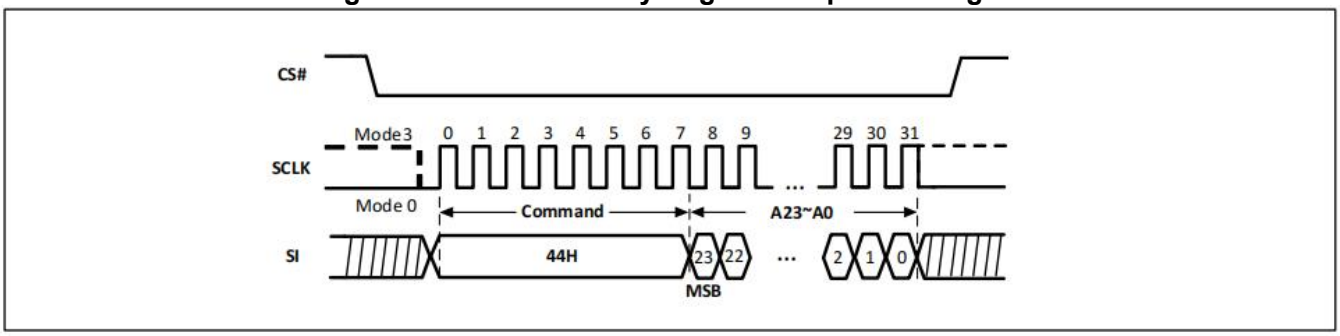
The ERSCUR command sequence is shown in Figure-25. The CS# pin must be driven high after the eighth bit of the last address byte is latched. If this is not done, the command will not be executed. After CS# is driven high, the self-timed ERSCUR operation will commence for a time duration of tSE.

While the Erase Security Register cycle is in progress, the Read Status Register command (05H) may still be accessed for checking the value of the Write in Progress (WIP) bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Erase Security Register cycle has finished, the WEL bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register are OTP and can be used to protect the security registers. Once the LB bit is set to 1, the corresponding security register will be permanently locked, and an ERSCUR command to that register will be ignored.

Table-11.1 Erase Security Register Address

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0001	00	Don't care
Security Register #2	00h	0010	00	Don't care
Security Register #3	00h	0011	00	Don't care

Figure-25. Erase Security Register Sequence Diagram



4.25 Program Security Register (PRSCUR) (42H)

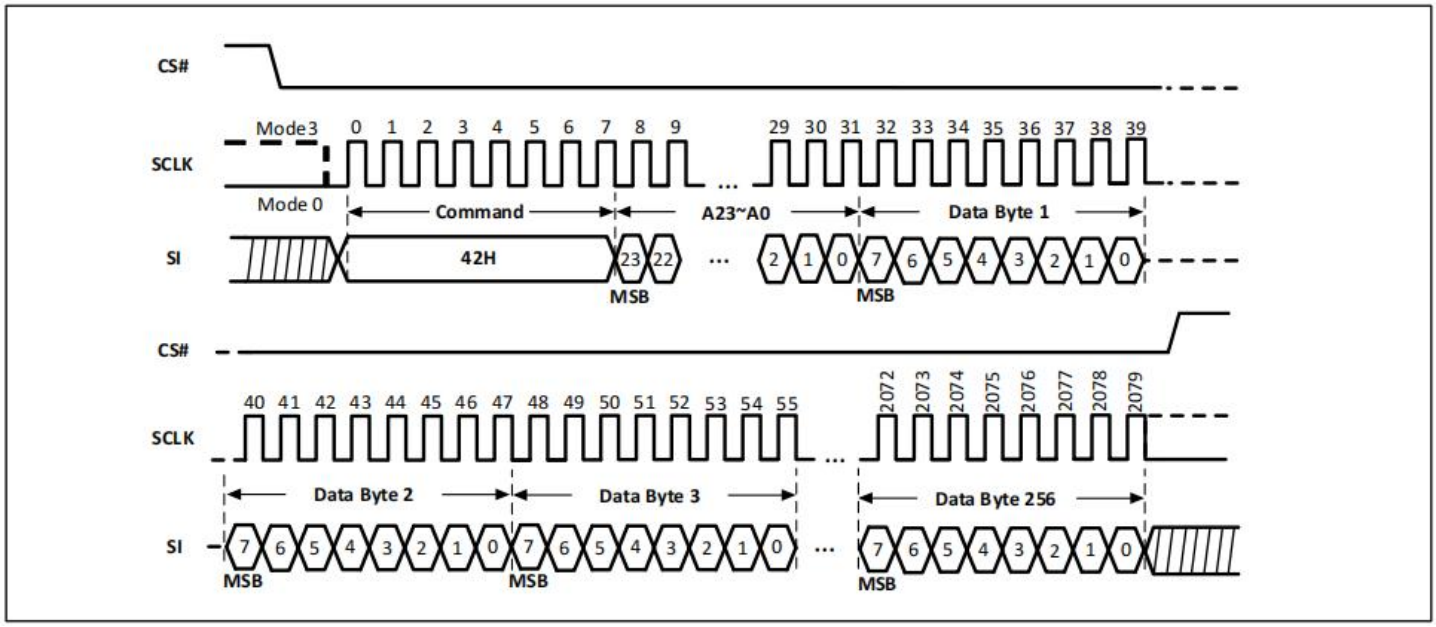
The Program Security Register (42H) command is similar to the Page Program (02H) command. It allows from one byte to 1024 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable (06H) command must be executed before the device will accept the PRSCUR Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the command code "42H" followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device.

The PRSCUR command sequence is shown in Figure-26. The Security Register Lock Bits (LB3-1) in the Status Register are OTP can be used to protect the security registers. Once Security Register Lock Bit (LB3-1) is set to 1, the corresponding security register will be permanently locked, and a PRSCUR command to that register will be ignored.

Table-11.2 Program Security Register Address

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0001	00	Byte Address
Security Register #2	00h	0010	00	Byte Address
Security Register #3	00h	0011	00	Byte Address

Figure-26. Program Security Register Sequence Diagram



4.26 Read Security Register (RDSCUR) (48H)

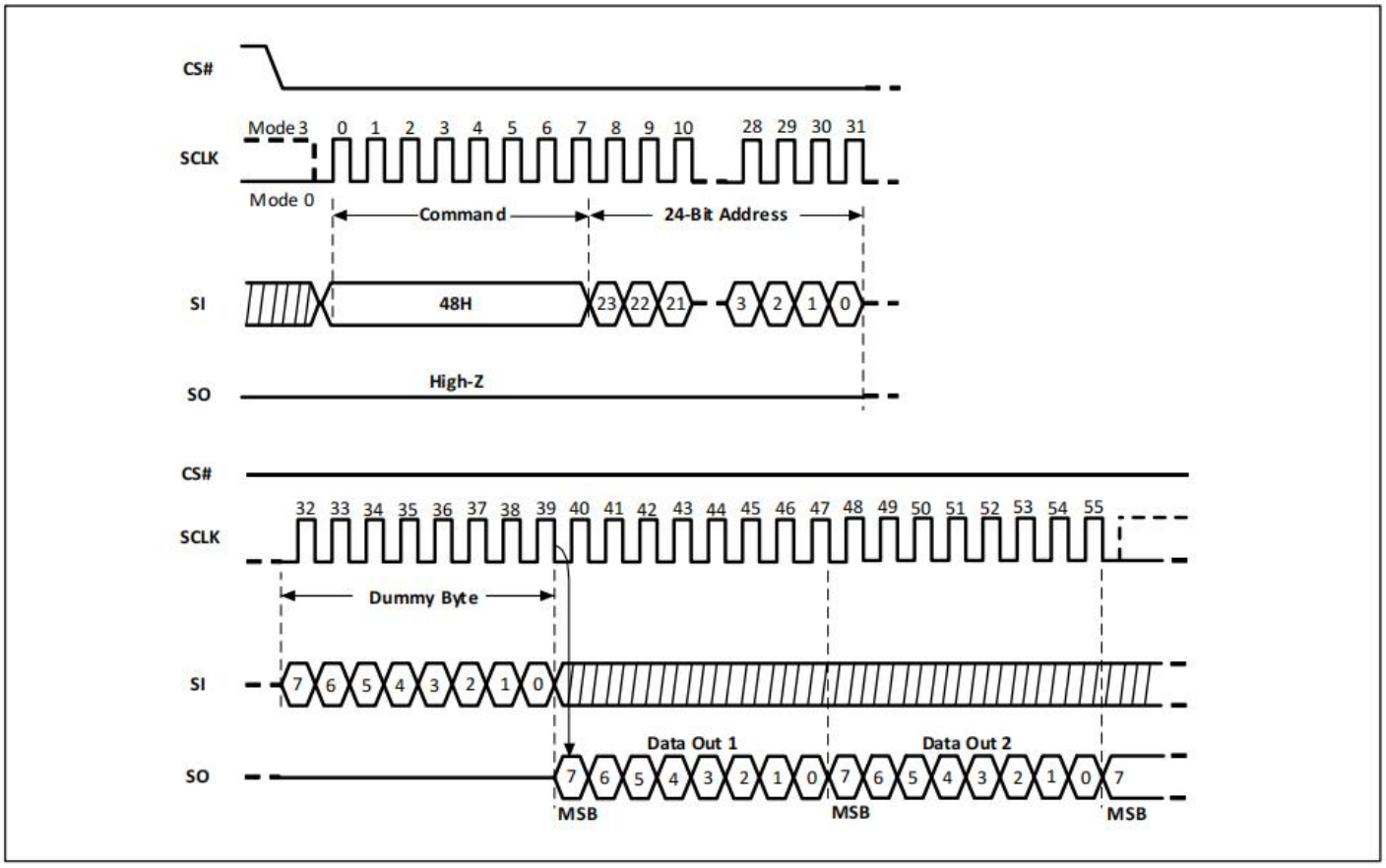
The Read Security Register (48H) command is similar to the Fast Read (0BH) command and allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the CS# pin low and then shifting the command code “48H” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, and following the eight dummy cycles, the data byte of the addressed memory location will be shifted out on the SO pin on the falling edge of SCLK with the most significant bit (MSB) first. The first byte addressed can be at any location. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte 3FFh), it will reset to 000h, the first byte of the register, and continue to increment. The command is completed by driving CS# high.

The RDSCUR command sequence is shown in Figure-27. If a RDSCUR command is issued while an Erase, Program, or Write cycle is in process (Write in Progress (WIP)=1), the command is ignored and will not have any effect on the current cycle. The RDSCUR command allows each bit being shifted out on SO pin at a Max frequency fC, on the falling edge of SCLK.

Table-11.3 Read Security Register Address

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0001	00	Byte Address
Security Register #2	00h	0010	00	Byte Address
Security Register #3	00h	0011	00	Byte Address

Figure-27. Read Security Register Sequence Diagram



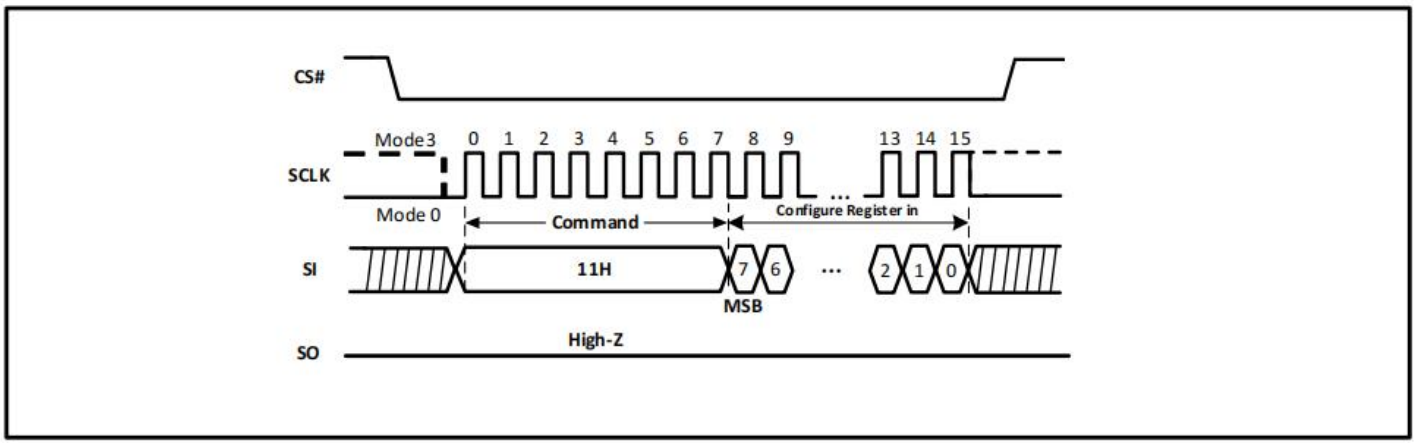
4.27 Write Configure Register (WRCR)(11H)

The Write Configure Register (WRCR) command allows new values to be written to the Configure Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The sequence of issuing WRCR instruction is: CS# goes low→ sending WRCR instruction code→ Configure Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Configure Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure-28. Write Configure Register (WRCR) Sequence (Command 11H)

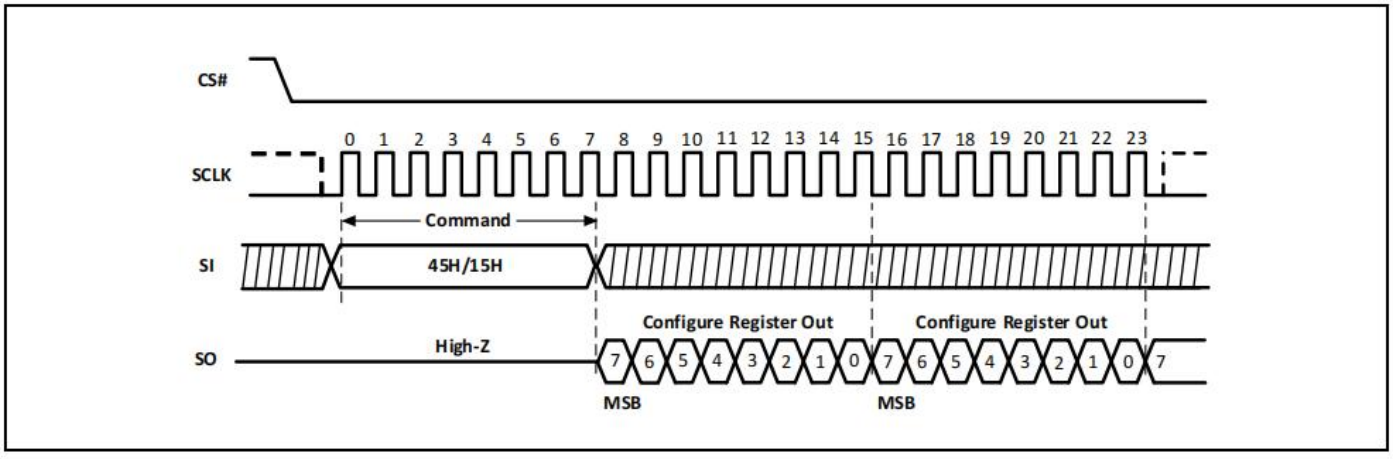


4.28 Read Configure Register (RDCR) (45H or 15H in SPI Mode)

The RDCR instruction is for reading Configure Register Bits. The Read Configure Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configure Register data out on SO.

Figure-29. Read Configure Register (Command 45H or 15H)



4.29 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (B9H) command is the only way to place the device in the lowest power consumption mode (the Deep Power-Down mode). It can also be used as an extra software protection mechanisms the device is not in active use, all Write, Program and Erase commands are ignored.

Driving Chip Select (CS#) High deselects the device and puts the device in the Standby mode (if there is no internal cycle currently in progress). However, Standby mode is not the Deep Power-Down mode. The Deep Power-Down mode can only be entered by executing the DP command, to reduce the standby current (from ISB1 to ISB2).

Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release from Deep Power-Down, Read Electronic Signature (ABH) command. This command releases the device from this mode and also outputs the Device ID on Data Output (SO).

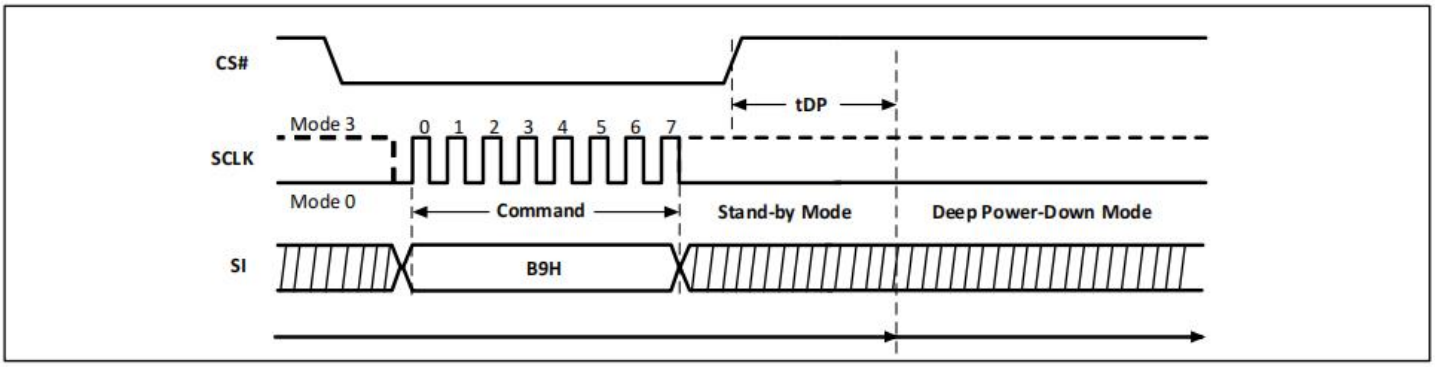
The Deep Power-Down mode automatically stops at Power-Down, and the device always Powers-up in the Standby mode. The DP command is entered by driving CS# Low, followed by the command code on Data

Input (SI). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-30. CS# must be driven High after the eighth bit of the command code has been latched in, otherwise the Deep Power-Down (B9H) command is not executed. As soon as CS# is driven High, a delay of tDP occurs before the supply current is reduced to ISB2 and the Deep Power-Down mode is entered.

Any DP command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-30. Deep Power-Down Sequence Diagram



4.30 Release form Deep Power-Down (RDP), Read Electronic Signature (RES) (ABH)

Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release from Deep Power-Down, Read Electronic Signature (ABH) command. Executing this command takes the device out of the Deep Power-Down mode.

Please note that this is not the same as or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identification (9FH) command. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identification command.

When used only to release the device from the power-down state, the command is issued by driving the Chip Select (CS#) pin low, shifting the command code “ABH” and driving CS# high as shown in Figure-31. After the time duration of tRES1 the device will resume normal operation and other commands will be accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the command is initiated by driving the CS# pin low and shifting the command code “ABH” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in Figure-32. The Device ID values are listed in "Tables of ID Definition" (Table-9). The Device ID can be read continuously. The command is completed by driving CS# high.

When CS# is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-Down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-Down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and CS# must remain High for at least tRES2 (max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute commands.

Except while an Erase, Program or Write Status Register cycle is in progress, the RDP, RES command always provides access to the 8-bit Device ID of the device and can be applied even if the Deep Power-Down mode has not been entered.

Any RDP, RES command issued to the device while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

Figure-31. Release from Deep Power-Down (RDP) Sequence Diagram

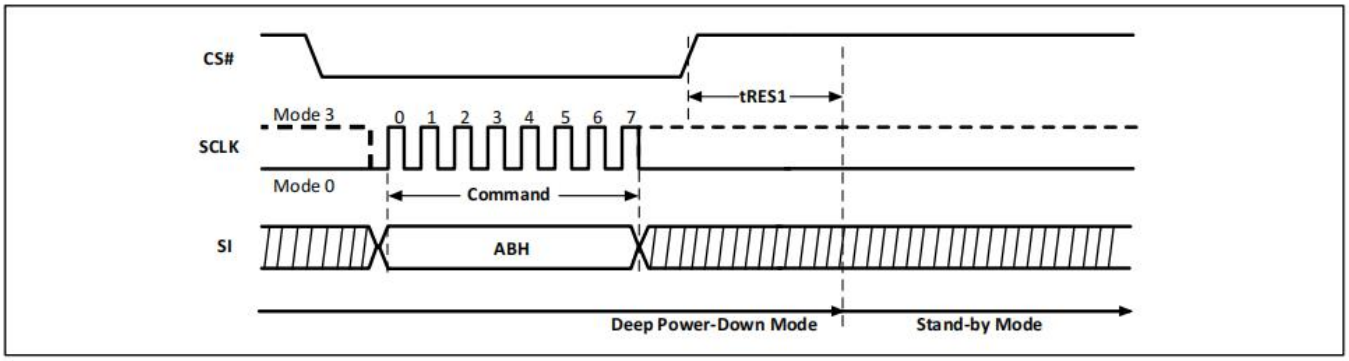
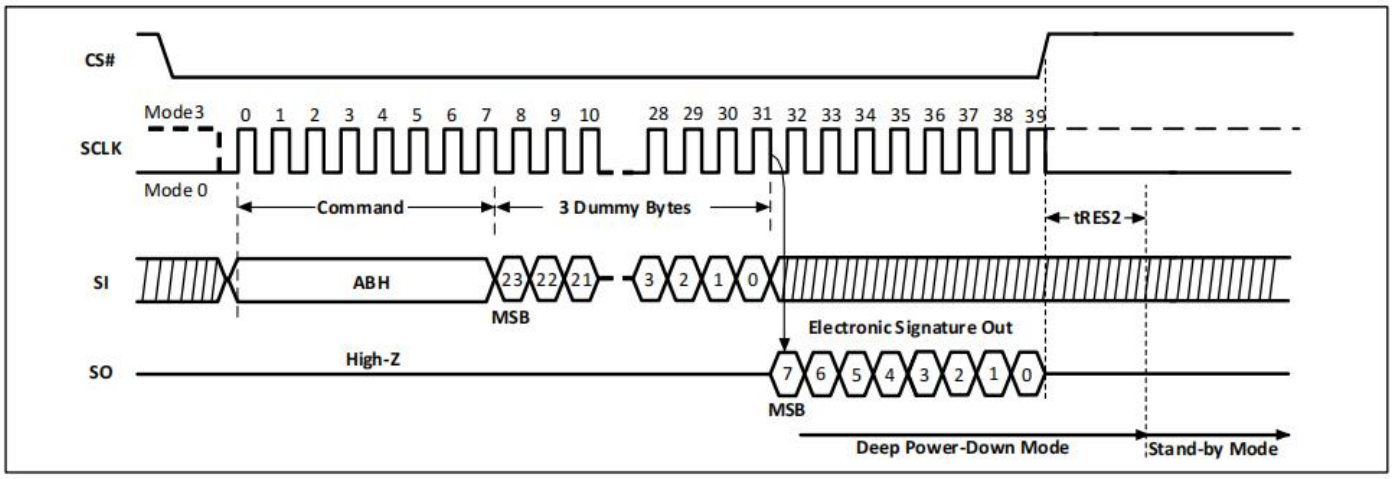


Figure-32. Read Electronic Signature (RES) Sequence Diagram

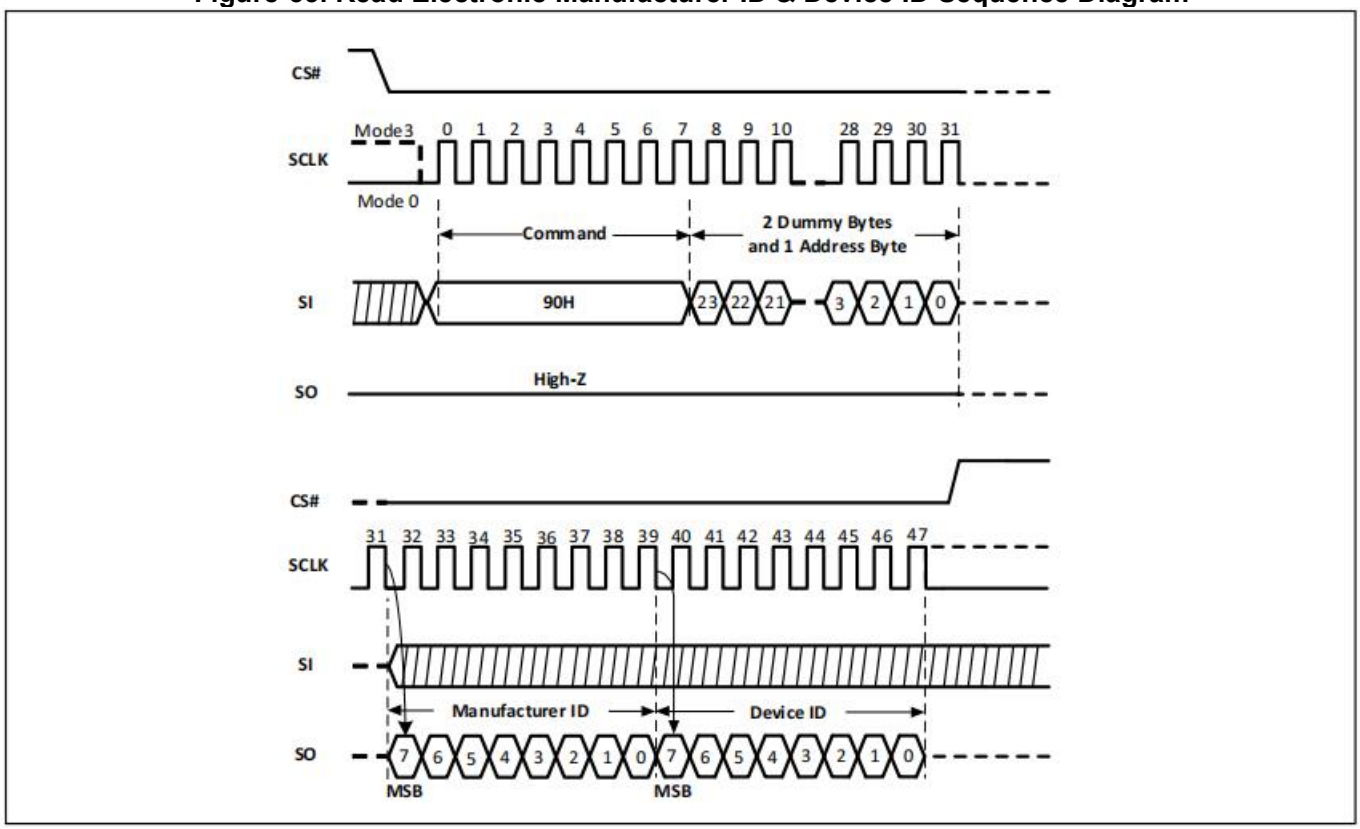


4.31 Read Electronic Manufacturer ID & Device ID (REMS) (90H)

The Read Electronic Manufacturer & Device ID (90H) command provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The REMS command is initiated by driving the CS# pin low and shifting the command code “90H” followed by two dummy bytes and one address byte (A7~A0). After which, the Manufacturer ID for ZETTA (BAh) and the Device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in Figure-33. The Device ID values are listed in "Tables of ID Definition" (Table-9). If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

Figure-33. Read Electronic Manufacturer ID & Device ID Sequence Diagram

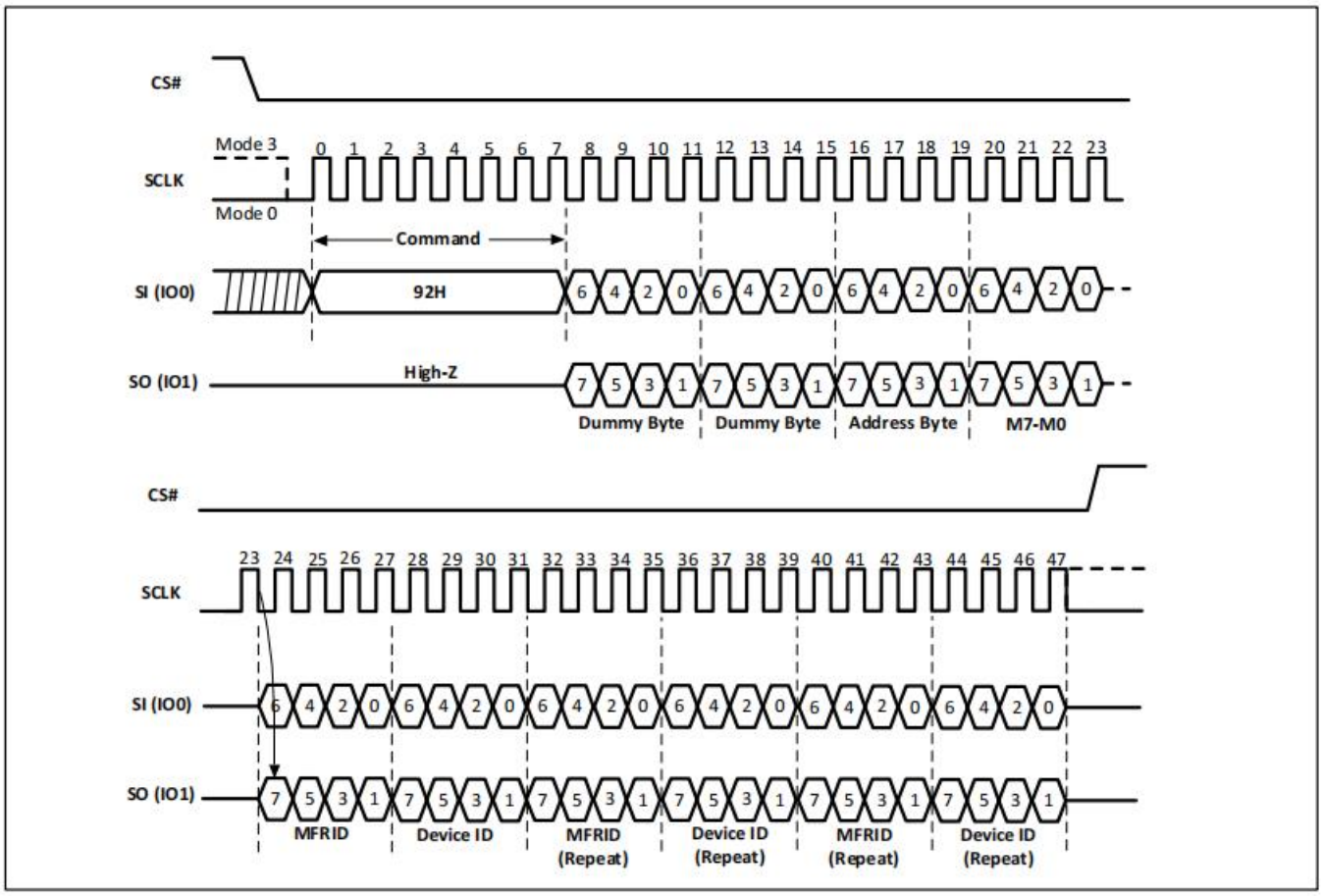


4.32 Dual I/O Read Electronic Manufacturer ID & Device ID (DREMS) (92H)

The Dual I/O Read Electronic Manufacturer ID & Device ID (92H) command is similar to the Read Electronic Manufacturer & Device ID (90H) command and returns the JEDEC assigned Manufacturer ID which uses two pins: IO0, IO1 as address input and ID output I/O.

The DREMS command is initiated by driving the CS# pin low and shifting the DREMS command code "92h" followed by two dummy bytes, one address byte (A7~A0). After which, the Manufacturer ID for ZETTA (BAh) and the Device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the one-byte address is initially set to 01h, then the device ID will be read first and followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The DREMS command is completed by driving CS# high.

Figure-34. Dual I/O Read Electronic Manufacturer ID & Device ID Sequence Diagram

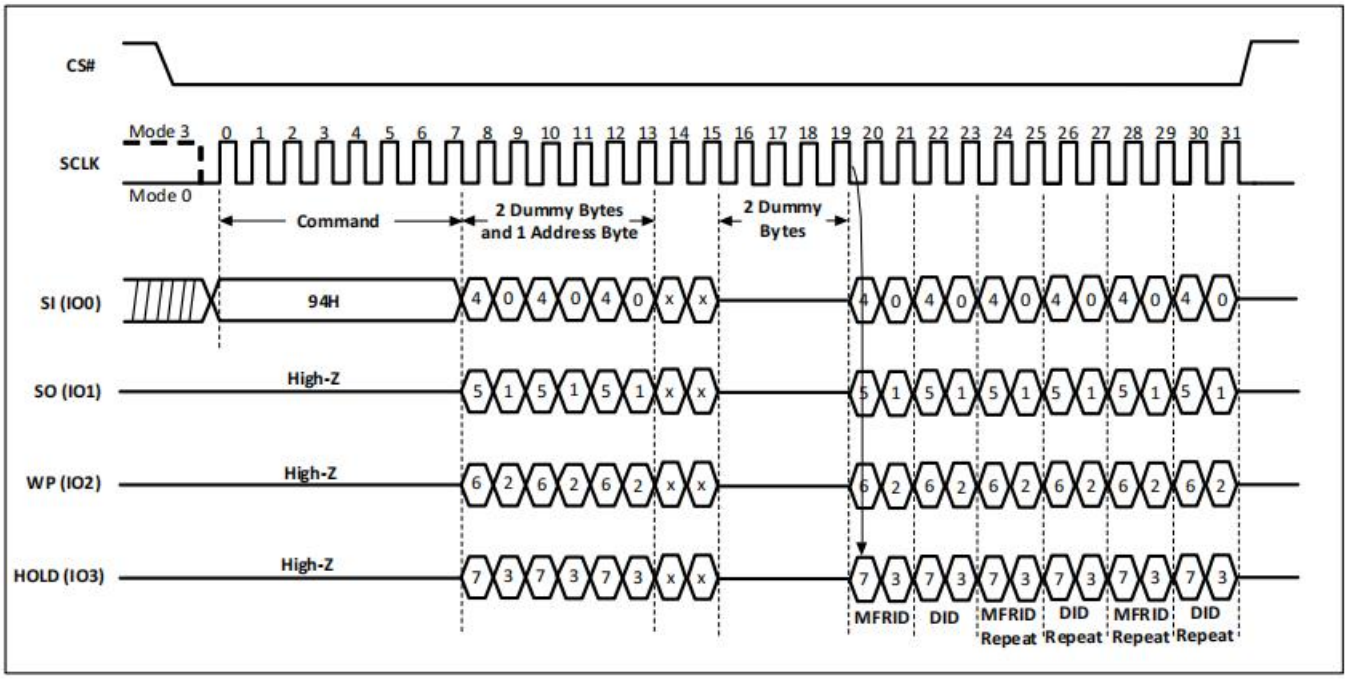


4.33 Quad I/O Read Electronic Manufacturer ID & Device ID (QREMS) (94H)

The Quad I/O Read Electronic Manufacturer ID & Device ID (94H) command is similar to the Read Electronic Manufacturer & Device ID (90H) command and returns the JEDEC assigned Manufacturer ID which uses four pins: IO0, IO1, IO2, IO3 as address input and ID output I/O. A Quad Enable (QE) of Status Register-2 must be executed before the device will accept the QREMS Command (The QE bit must equal "1").

The QREMS command is initiated by driving the CS# pin low and shifting the QREMS command code "94h" followed by two dummy bytes, one address (A7~A0) byte, two dummy bytes. After which, the Manufacturer ID for ZETTA (BAh) and the Device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The QREMS command is completed by driving CS# high.

Figure-35. Quad I/O Read Electronic Manufacturer ID & Device ID Sequence Diagram



4.34 Read Identification (RDID) (9FH)

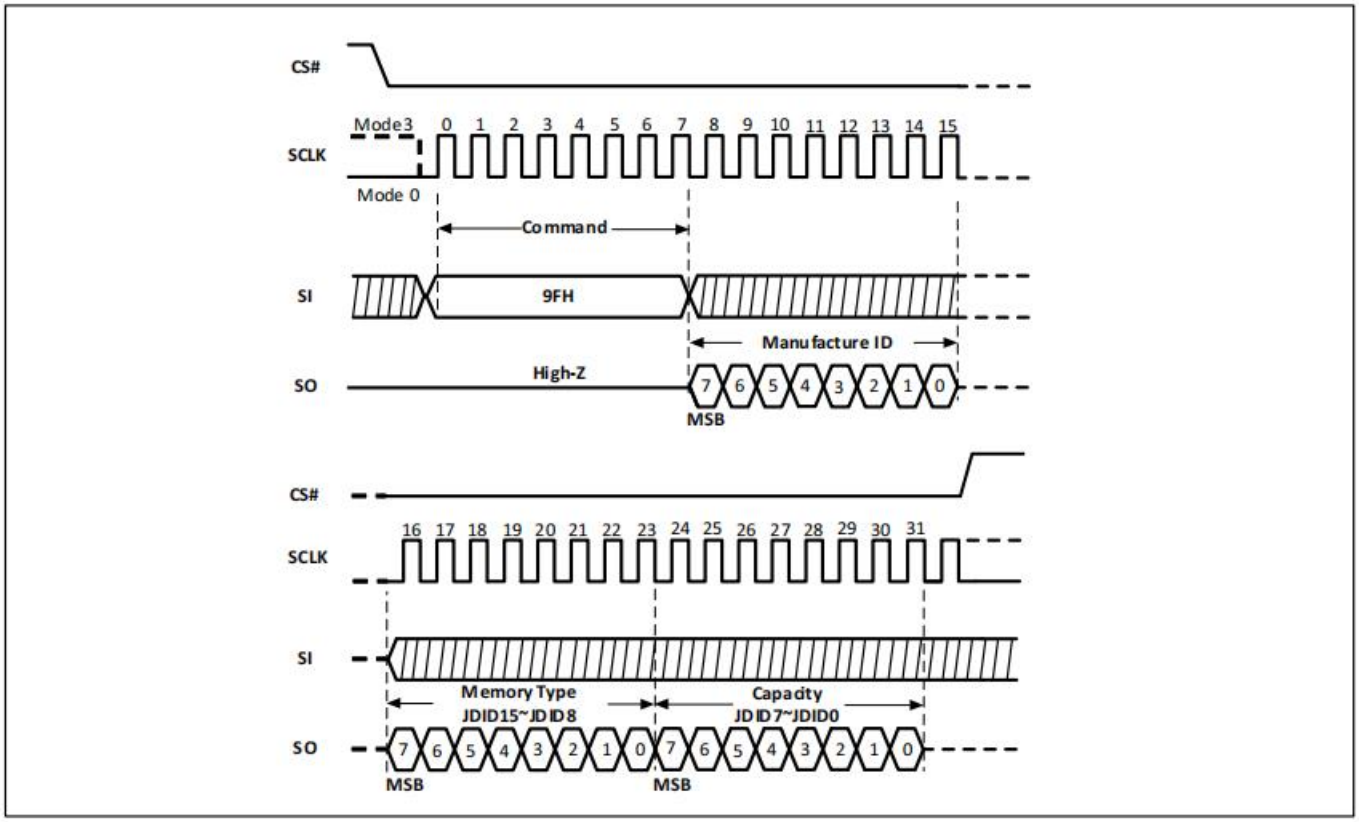
The Read Identification (9FH) command allows the 8-bit Manufacturer ID to be read, followed by two bytes of Device ID. The Device ID indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The ZETTA Manufacturer ID and Device ID are list as "Tables of ID Definition" (Table-9).

Any RDID command issued while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The RDID command should not be issued while the device is in Deep Power down mode.

The device is first selected by driving the CS# Low. Then the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification stored in the memory, shifted out on the SO pin on the falling edge of SCLK. The command sequence is shown in Figure-36. The RDID command is terminated by driving CS# High at any time during data output.

When CS# is driven High, the device is placed in the standby mode. Once in the standby stage, the device waits to be selected, so that it can receive, decode and execute commands.

Figure-36. Read Identification Sequence Diagram



4.35 Program/Erase Suspend/Resume (75H)

The Suspend (75H or B0H) command interrupts a Page Program, Page Erase, Sector Erase, Half Block Erase or Block Erase operation to allow access to the memory array. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the page, sector or block being erased.

Table-12.0 Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Page Erase	All but the Page being erased
Sector Erase(4KB)	All but the 4KB Sector being erased
Half Block Erase(32KB)	All but the 32KB Block being erased
Block Erase(64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend command, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS2 or SUS1 sets to “1”. Afterwards, the device is ready to accept one of the commands listed in Table-12.1 "Acceptable Commands During Program/Erase Suspend after tPSL/tESL" (e.g. Read Data Bytes at Higher Speed (0BH) command). Refer to "AC CHARACTERISTICS" for tPSL and tESL timings. Table-12.2 "Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, Read Status Register, Read Security Registers, Reset Enable and Reset can be issued at any time after the Suspend command.

Status Register bit 15 (SUS2) and bit 10 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to “1” when a program operation is suspended. The SUS1 (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The SUS2 or SUS1 clears to “0” when the program or erase operation is resumed.

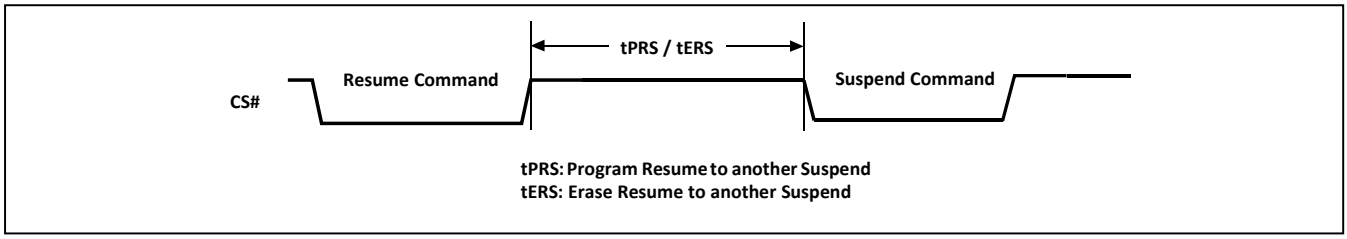
Table-12.1 Acceptable Commands During Program/Erase Suspend after tPSL/tESL

Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03H	•	•
FAST READ	0BH	•	•
DREAD	3BH	•	•
QREAD	6BH	•	•
2READ	BBH	•	•
4READ	EBH	•	•
RDSFDP	5AH	•	•
RDID	9FH	•	•
REMS	90H	•	•
DREMS	92H	•	•
QREMS	94H	•	•
RDSCUR	48H	•	•
SBL	77H	•	•
WREN	06H		•
RESUME	7AH OR 30H	•	•
PP	02H		•
DPP	A2H		•
QPP	32H		•

Table-12.2 Acceptable Commands During Suspend（tPSL/tESL not required）

Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04H	•	•
RDSR	05H	•	•
RDSR2	35H	•	•
ASI	25H	•	•
RSTEN	66H	•	•
RST	99H	•	•
NOP	00H	•	•

Figure-37. Resume to Suspend Latency

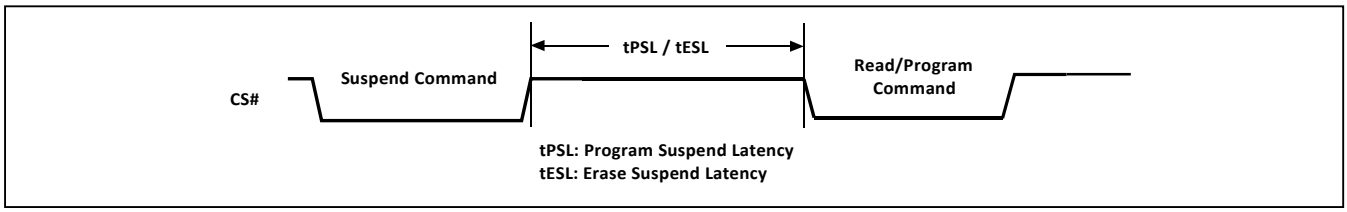


Erase Suspend to Program

The “Erase Suspend to Program” feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (06H) command must be issued before any Page Program (02H) command.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The Write Enable Latch (WEL) and Write in Progress (WIP) bits of the Status Register will remain “1” while the Page Program operation is in progress and will both clear to “0” when the Page Program operation completes.

Figure-38. Suspend to Read/Program Latency

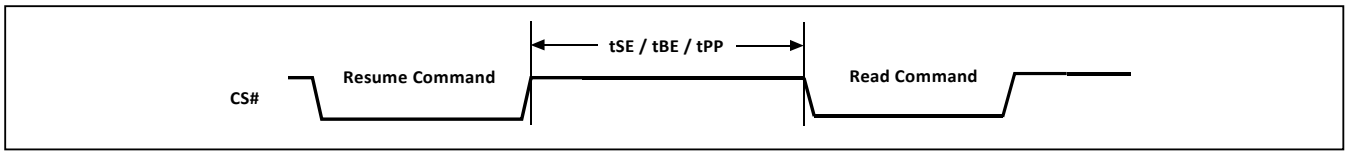


4.36 Program Resume and Erase Resume (7AH)

The Resume (7AH or 30H) command resumes a suspended Page Program, Page Erase, Sector Erase, Half Block Erase or Block Erase operation. Before issuing the Resume command to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume command, the Write Enable Latch (WEL) and Write in Progress (WIP) bits are set to “1” and the SUS2 or SUS1 is cleared to “0”. The program or erase operation will continue until finished ("Resume to Read Latency") or until another Suspend (75H or B0H) command is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend command ("Resume to Suspend Latency").

Figure-39. Program Resume and Erase Resume Sequence Diagram

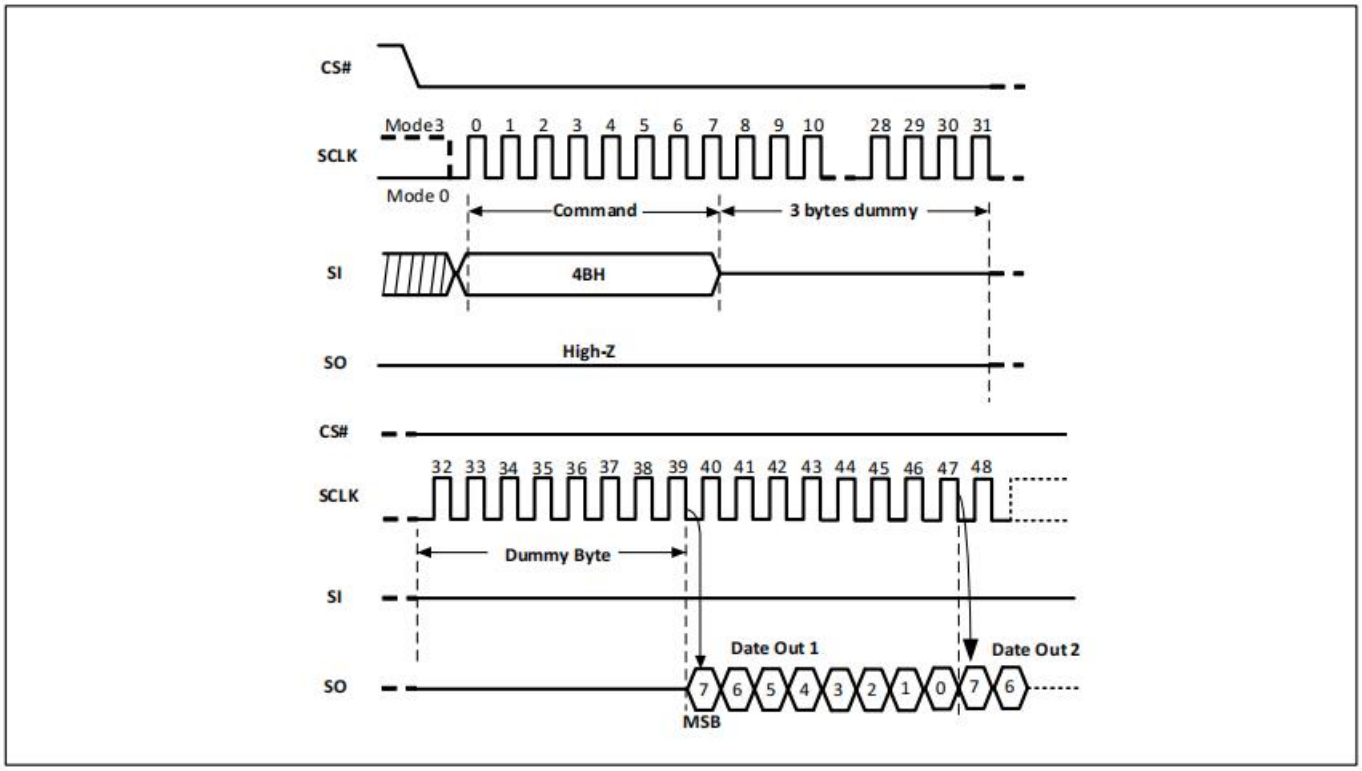


4.37 Read Unique ID (RUID) (4BH)

The Read Unique ID (4BH) command accesses a factory-set read-only 128-bit number that is unique to each ZD25WQ32C device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The RUID command is initiated by driving the CS# pin low and shifting the command code “4BH” followed by four dummy bytes. Then, the 128-bit ID is shifted out on the falling edge of SCLK as shown in Figure-40.

Figure-40. Read Unique ID Sequence Diagram



4.38 Read SFDP Mode (RDSFDP) (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be queried by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a JEDEC Standard, JESD216B.

ZD25WQ32C features the Read SFDP Mode (5AH) command. The host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.

The device is first selected by driving Chip Select (CS#) Low. The command code for the RDSFDP is followed by a 3-byte address (A23~A0) and a dummy byte, with each bit latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at the specified address, is shifted out on Data Output (SO) at a maximum frequency fC on the falling edge of SCLK.

The command sequence is shown in Figure-41. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The entire SFDP table can, therefore, be read with a single RDSFDP command. When the highest address is reached, the address counter rolls over to 0x00h, allowing the read sequence to be continued indefinitely. The RDSFDP command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any RDSFDP commands issued, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-41. Read Serial Flash Discoverable Parameter Sequence Diagram

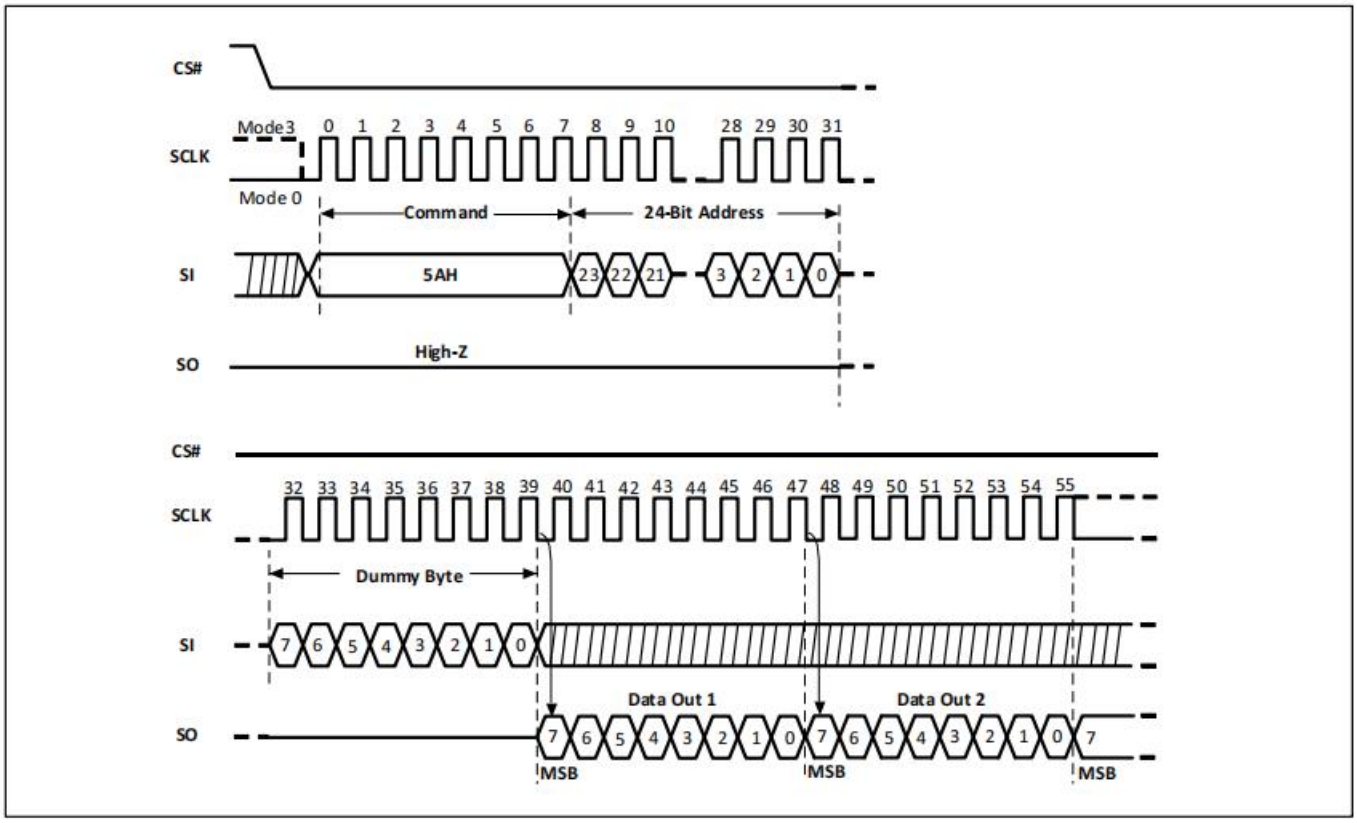


Table-13. Serial Flash Discoverable Parameter (SFDP) Table

Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed: 50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (ZETTA Device Manufacturer ID)	It is indicates ZETTA manufacturer ID	10H	07:00	BAH	BAH
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of ZETTA Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3 Byte only, 01: 3 or 4 Byte, 10: 4 Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	01FFFFFFH	
(1-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1-1-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H

Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	Data
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support	3CH	07:05	000b	08H
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3EH	20:16	00000b	80H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	100b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	FFH	FFH
Unused		45H:44H	15:00	FFH	FFH
(2-2-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	FFH	FFH
(4-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	52H	23:16	08H	08H
Sector Type 4 erase Opcode		53H	31:24	81H	81H

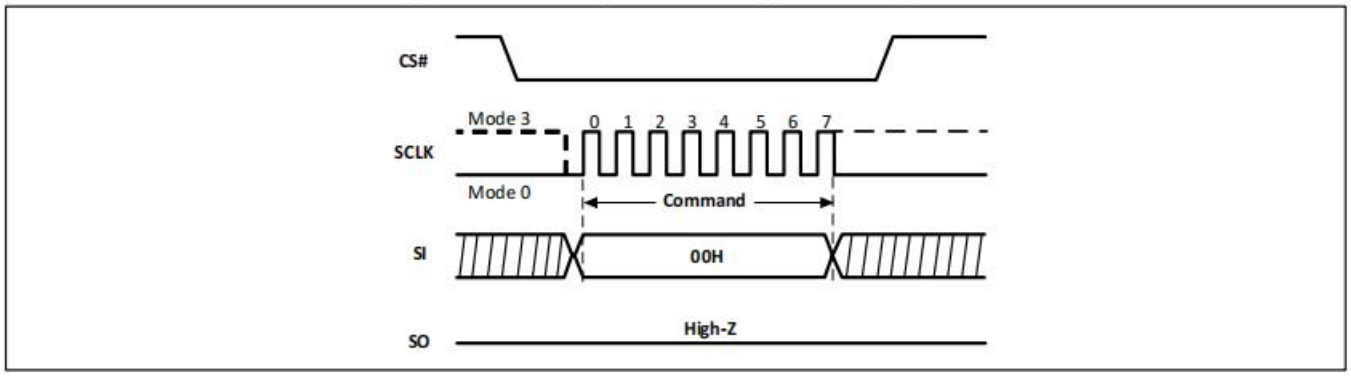
Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	1650H	1650H
HW Reset# pin	0=not support 1=support	65H:64H	00	0b	F99EH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable (66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B Wrap-Around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	0b	CBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

4.39 No Operation (NOP)

The No Operation (00H) command is only able to terminate the Reset Enable (66H) command and will not affect any other command.

The IO[3:1] are don't care.

Figure-42. No Operation Sequence Diagram

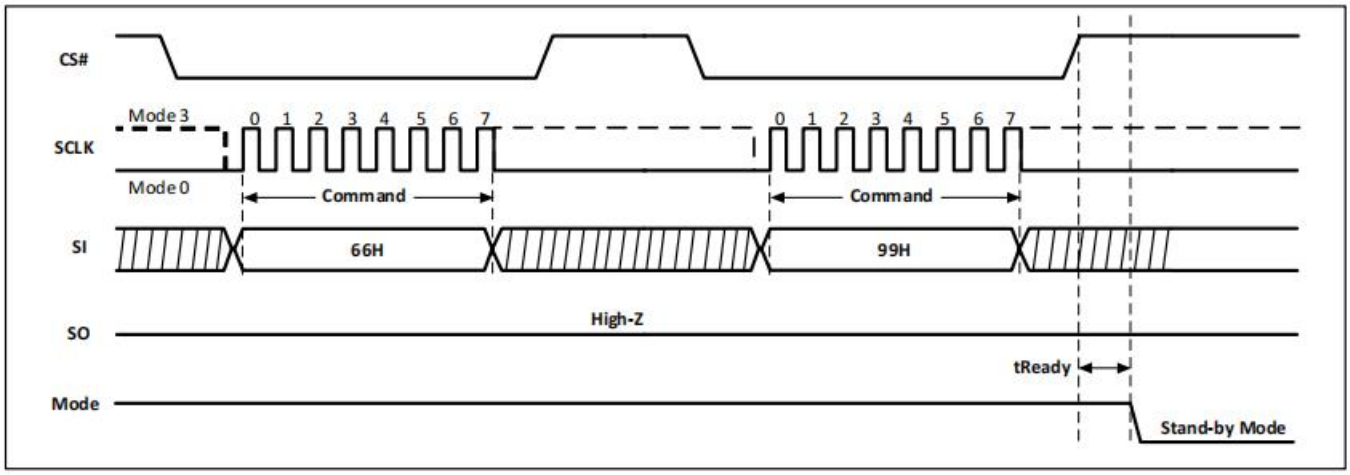


4.40 Reset Enable (RSTEN) (66H) and Reset (RST) (99H)

The Software Reset operation combines two commands: Reset Enable (66H) command and Reset (99H) command. It returns the device to standby mode. All the volatile bits and settings will be cleared which returns the device to the same default status as power on. The Reset command immediately following a Reset Enable command, initiates the Software Reset process. Any command other than Reset following the Reset Enable command, will clear the reset enable condition and prevent a later Reset command from being recognized.

If the Reset command is executed during a program or erase operation, the operation will be disabled and the data under processing could be damaged or lost.

Figure-43. Reset Enable and Reset Sequence Diagram



5. ELECTRICAL SPECIFICATIONS

5.1 Power-On Timing

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period oftVSL.

Figure-44. AC Timing at Device Power-Up

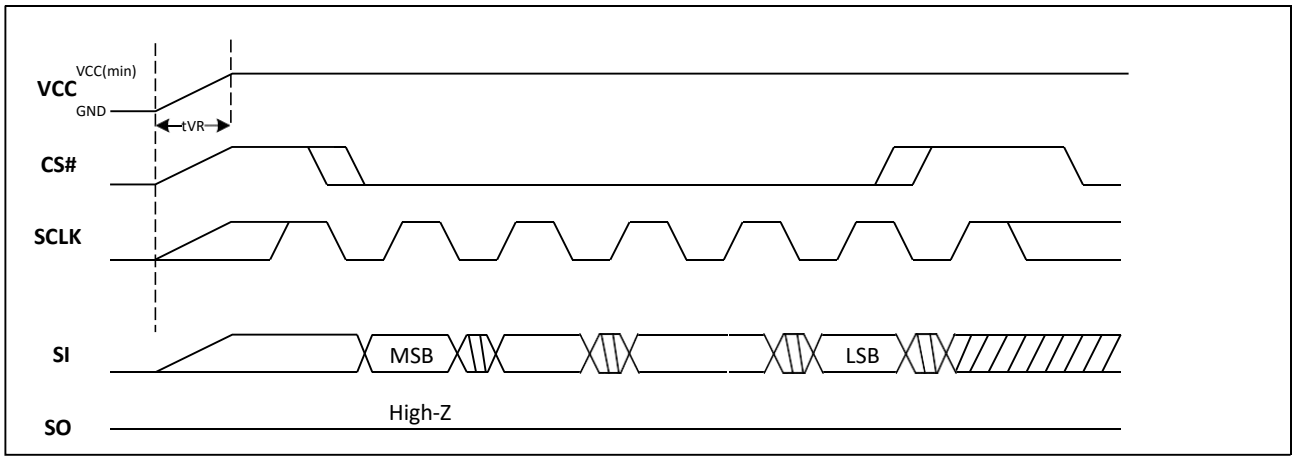


Figure-45. Power-On Timing Sequence Diagram

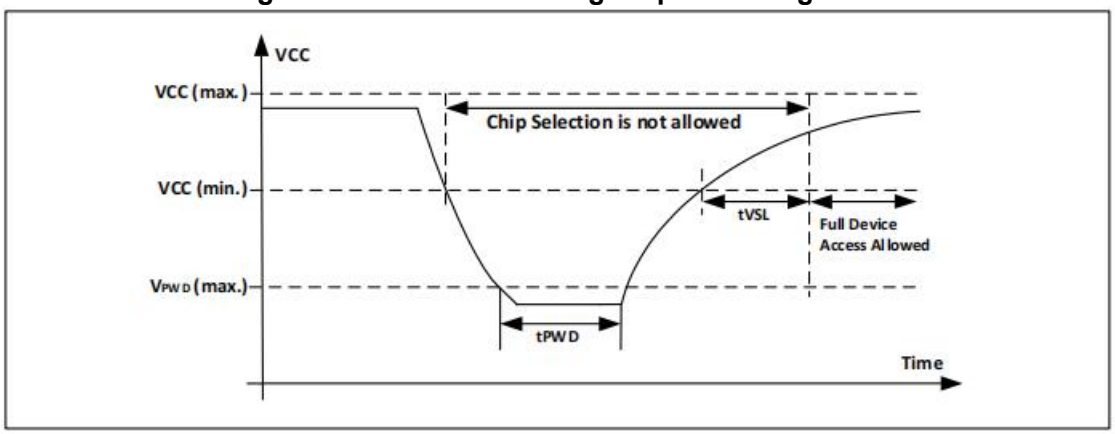


Table-14 Power-Up Timing and Write Inhibit Threshold

Sym.	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	0.3		ms
tVR	Vcc Rise Time	1	500000	Us/V
VWI	Write Inhibit Voltage	1	1.55	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1.1	V
tPWD	The minimum duration for ensuring initialization will occur	300		us

5.2 Initial Delivery State

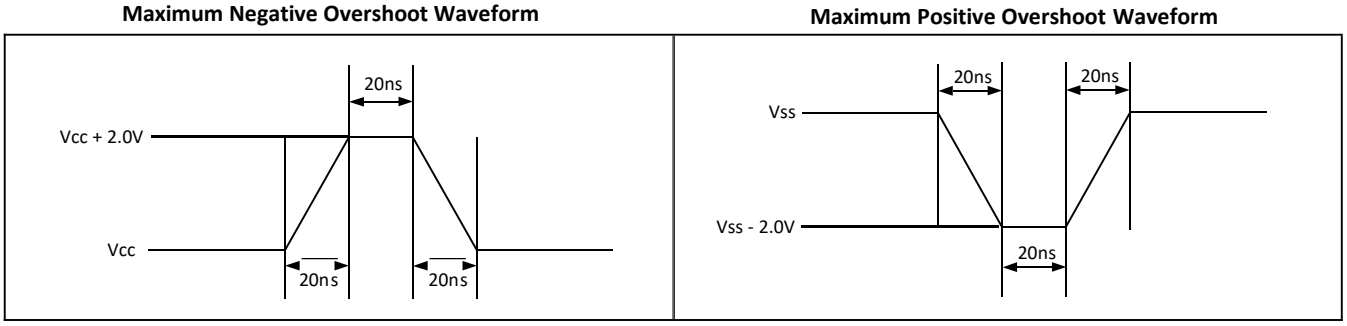
The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0)

5.3 Absolute Maximum Ratings

Table-15 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
Transient Input / Output Voltage(note: overshoot)	-2.0 to VCC+2.0	V
VCC	-0.6 to 4.2	V

Figure-46. Maximum Negative/positive Overshoot Diagram



5.4 AC Measurement Conditions

Table-16. AC Measurement Conditions

Sym.	Parameter	Min.	Typ.	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = GND
COUT	Output Capacitance			8	pF	VOUT = GND
CL	Load Capacitance		30		pF	
	Input			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC			

5.5 DC Characteristics

Table-17. DC Parameters (Ta=-40°C to +85°C)

Symbol	Parameter	Conditions	1.65V to 3.6V			2.3V to 3.6V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.1	3.0		0.2	3.0	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=Vcc all inputs at CMOS levels		4.5	18		7.5	18	uA
I_{CC1}	Low power read current (03h)	f=1MHz; IOUT=0mA		1.0	1.5		0.5	1.5	mA
		f=33MHz; IOUT=0mA		1.3	2.5		2.0	2.5	mA
I_{CC2}	Read current (0Bh)	f=50MHz; IOUT=0mA		1.3	4		2.0	4.5	mA
		f=86MHz; IOUT=0mA		2.0	4		2.0	4	mA
I_{CC3}	Program current	CS#=Vcc		1.3	4		2.5	3.5	mA
I_{CC4}	Erase current	CS#=Vcc		1.3	4		2.0	3.5	mA
I_{LI}	Input load current	All inputs at CMOS level			1.0			1.0	uA
I_{LO}	Output leakage	All inputs at CMOS level			1.0			1.0	uA
V_{IL}	Input low voltage				0.2Vcc			0.2Vcc	V
V_{IH}	Input high voltage		0.8Vcc			0.8Vcc			V
V_{OL}	Output low voltage	IOL=100uA			0.2			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			Vcc-0.2			V

Note:

1. Typical values measured at 1.8V @ 25°C for the 1.65V to 3.6V range.
2. Typical values measured at 3.0V @ 25°C for the 2.3V to 3.6V range.

5.6 AC Characteristics

Table-18. AC Parameters (Ta=-40°C to +85°C)

Symbol	Alt.	Parameter	1.65V~3.6V			2.3V~3.6V			Unit
			min.	typ	max.	min	typ	max	
fsclk	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE32K, BE, CE, DP,RES, WREN, WRDI, RDID, RDSR, WRSR(7)			66			104	MHz
fRSCLK	fR	Clock Frequency for READ instructions			40			50	MHz
fTSCLK	fT	Clock Frequency for DREAD instructions			66			86	MHz
		Clock Frequency for 2READinstructions			66			86	MHz
	fQ	Clock Frequency for QREAD instructions			66			86	MHz
		Clock Frequency for 4READ instructions			66			86	MHz
fQPP		Clock Frequency for QPP (Quad page program)			66			86	MHz
tCH(1)	tCLH	Clock High Time	6			4.5			ns
tCL(1)	tCLL	Clock Low Time (fSCLK) 45% x (1fSCLK)	6			4.5			ns
tCLCH(7)		Clock Rise Time (peak to peak)	0.1			0.1			v/ns
tCHCL(7)		Clock Fall Time (peak to peak)	0.1			0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	6.5			5.5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			5			ns
tDVCH	tDSU	Data In Setup Time	4			3			ns
tCHDX	tDH	Data In Hold Time	3			3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	10			8			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	6			6			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	25			25			ns
		CS# Deselect Time From Write,Erase,Program to Read Status Register	30			30			ns
		Volatile Status Register Write Time	45			45			ns
tSHQZ(7)	tDIS	Output Disable Time			6			6	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			14			8	ns
		Clock Low to Output Valid Loading 15pF			12			7	ns
tCLQX	tHO	Output Hold Time	0			0			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	6			6			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	6			6			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	5			5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			6			6	ns
tHLQZ	tHZ	HOLD# to Output High-Z			6			6	ns
tWHSL(3)		Write Protect Setup Time	23			23			ns
tSHWL(3)		Write Protect Hold Time	105			105			ns
tDP		CS# High to Deep Power-down Mode			3			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			8			8	us
tRES2		CS# High To Standby Mode With Electronic Signature Read			8			8	us
tW		Write Status Register Cycle Time		10	20		10	20	ms
tReady		Reset recovery time(for erase/program operation except WRSR)	40			40			us
		Reset recovery time(for WRSR operation)		10	20		10	20	ms

Table-19. AC Parameters for Program and Erase(Ta=-40°C to +85°C)

Sym.	Parameter	1.65V to 3.6V			Units
		Min.	Typ.	Max.	
$T_{ESL(6)}$	Erase Suspend Latency			30	us
$T_{PSL(6)}$	Program Suspend Latency			30	us
$T_{PRS(4)}$	Latency between Program Resume and next Suspend	0.3			us
$T_{ERS(5)}$	Latency between Erase Resume and next Suspend	0.3			us
t_{PP}	Page program time (up to 256 bytes)		2	3	ms
t_{PE}	Page erase time		10	20	ms
t_{SE}	Sector erase time		10	20	ms
t_{BE1}	Block erase time for 32K bytes		10	20	ms
t_{BE2}	Block erase time for 64K bytes		10	20	ms
t_{CE}	Chip erase time		10	20	ms

Notes:

1. tCH + tCLmust be greater than or equal to 1/Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR command.
4. Program operation may be interrupted as often as system request. The minimum timing of tPRS must be observed before issuing the next program suspend command. However, for a Program operation to make progress, tPRS ≥ 100us must be included in resume-to-suspend loop(s). Not 100% tested.
5. Erase operation may be interrupted as often as system request. The minimum timing of tERS must be observed before issuing the next erase suspend command. However, in order for an Erase operation to make progress, tERS ≥ 200us must be included in resume-to-suspend loop(s). Notes. Not 100% tested.
6. Latency time is required to complete Erase/Program Suspend operation.
7. The value guaranteed by characterization, not 100% tested in production.

Figure-47. Serial Input Timing

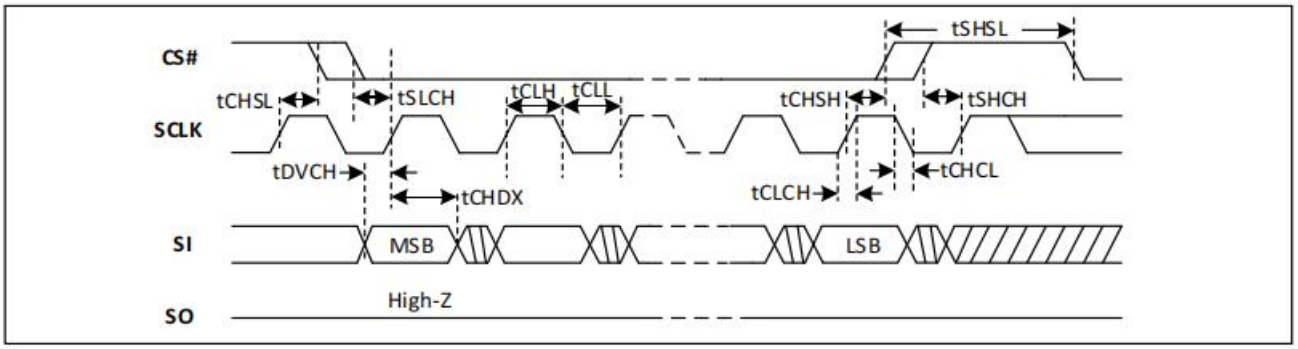


Figure-48. Output Timing

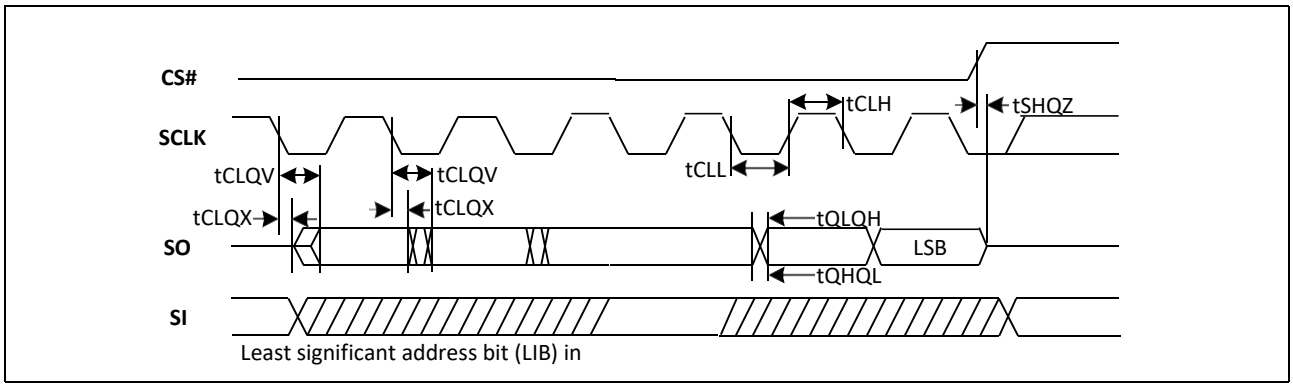


Figure-49. Hold Timing

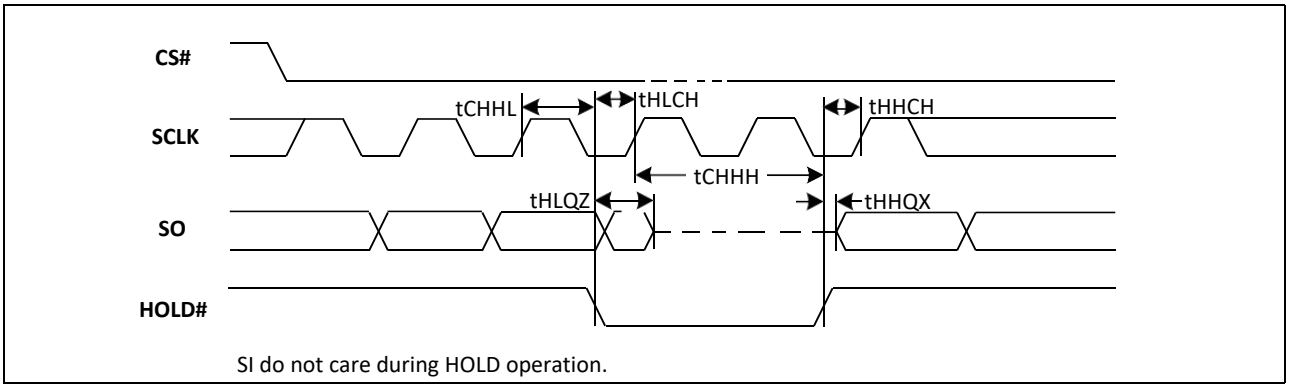
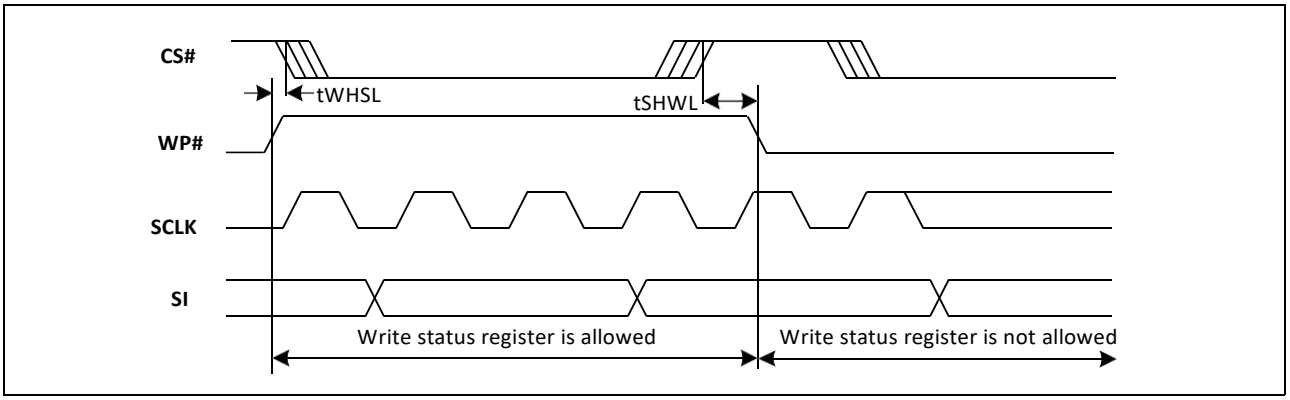
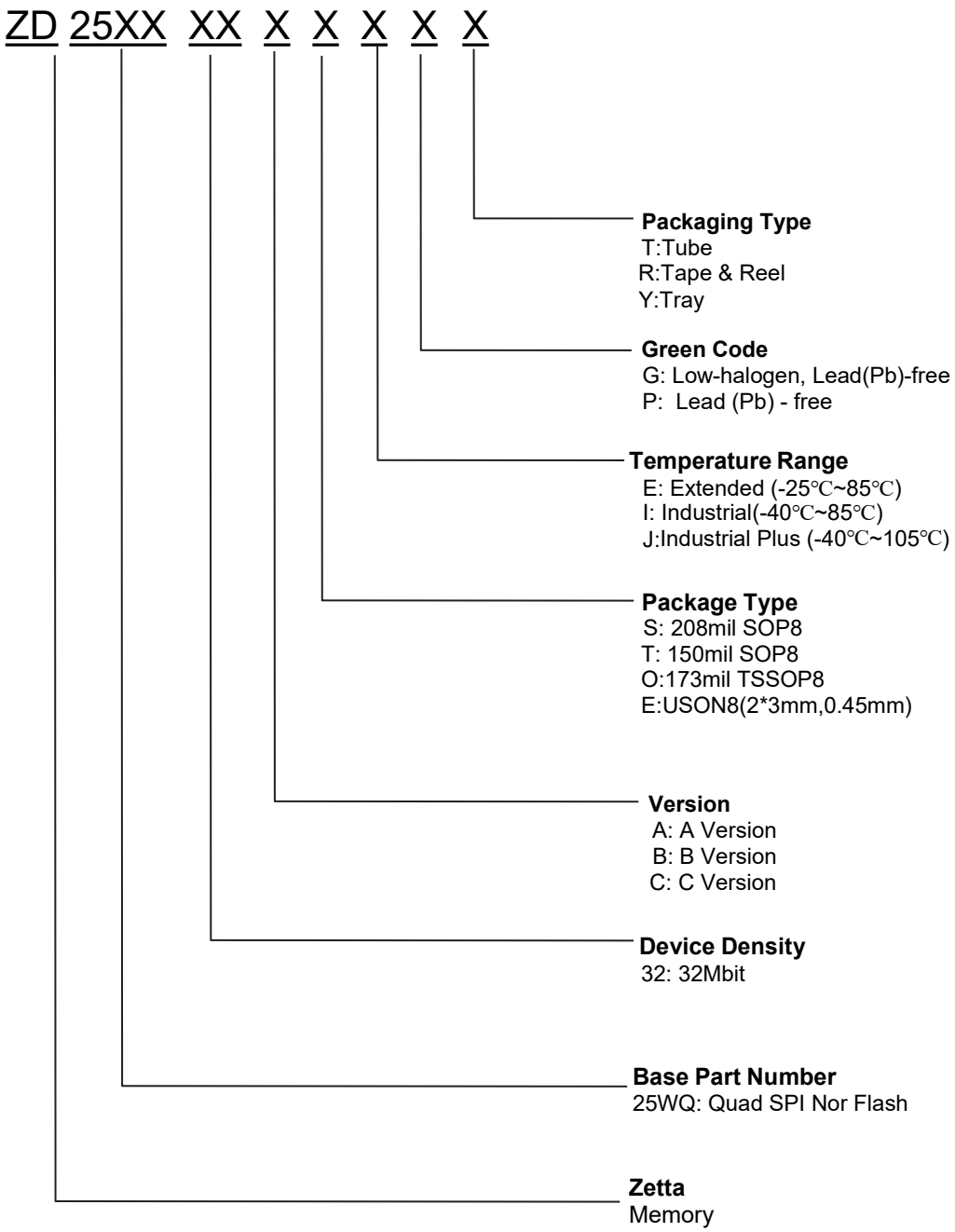


Figure-50. WP Timing

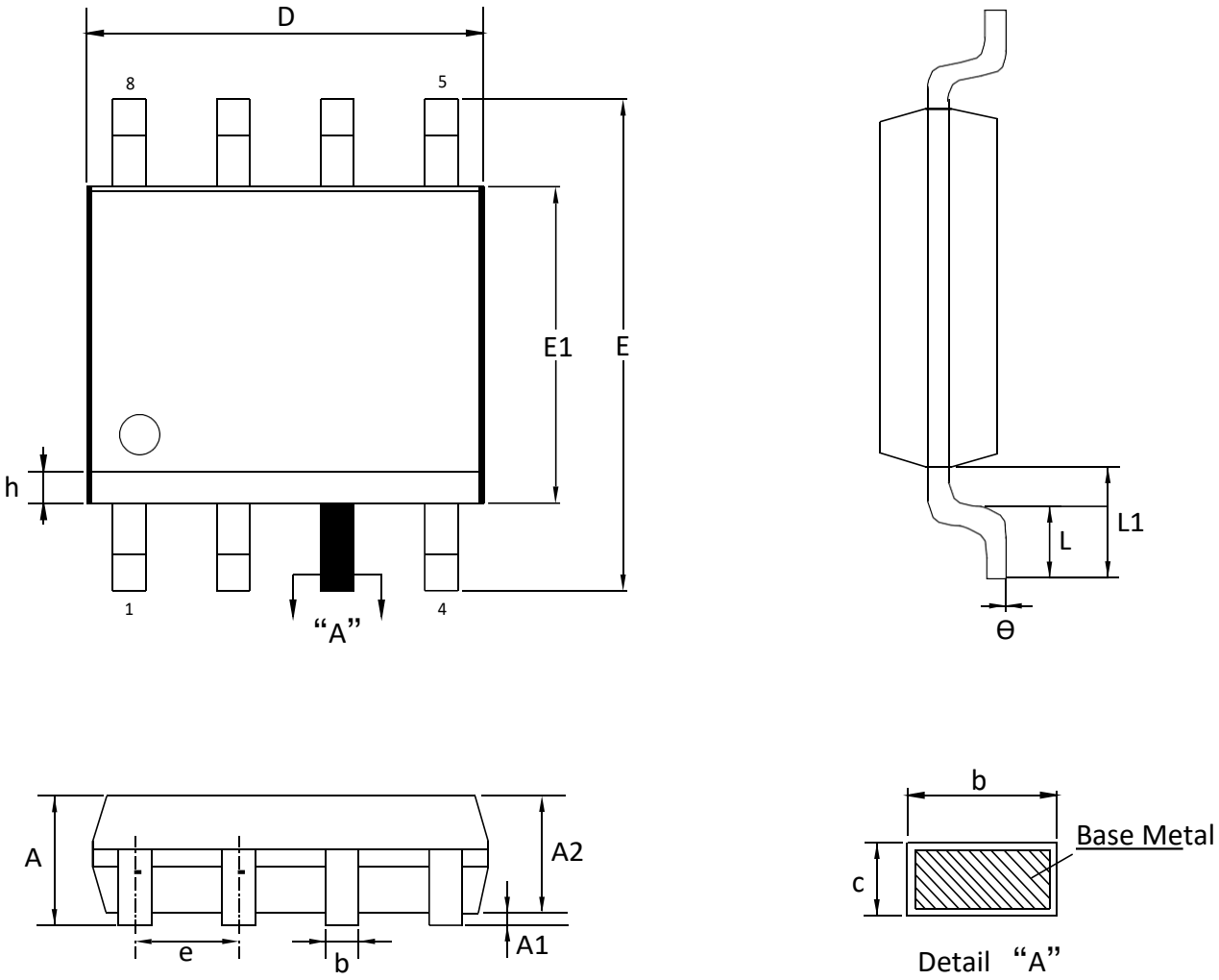


6. ORDERING INFORMATION



7.PACKAGE INFORMATION

7.1 Package SOP8 150MIL



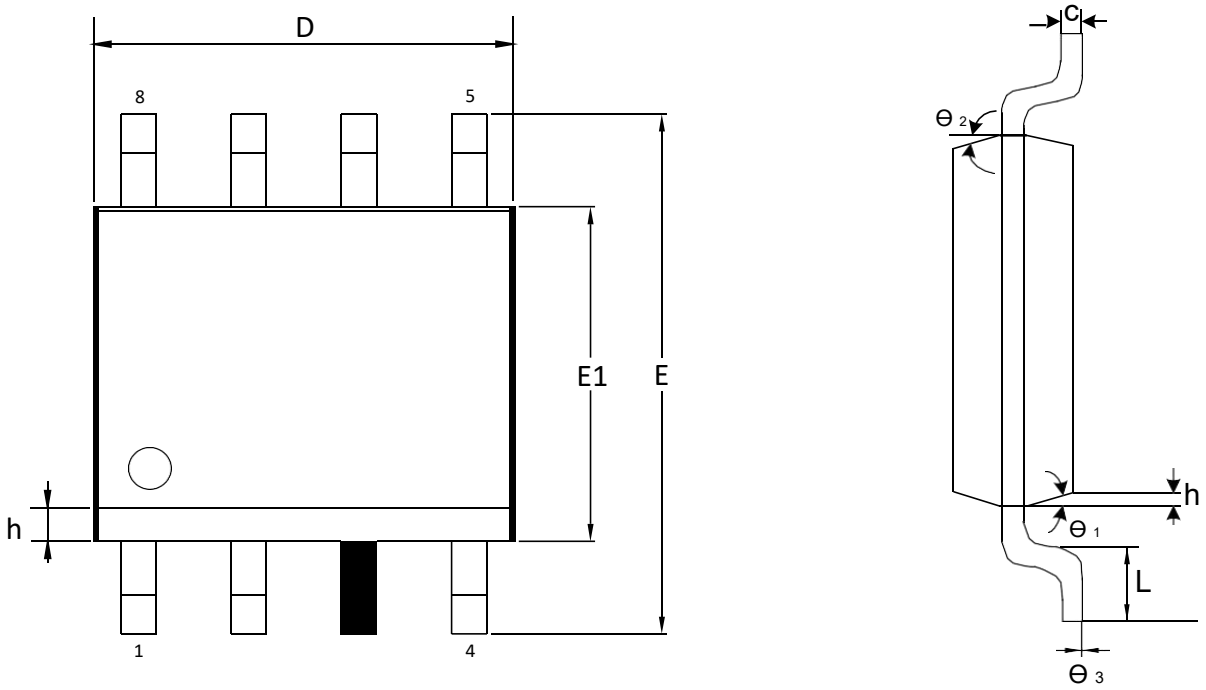
Dimensions

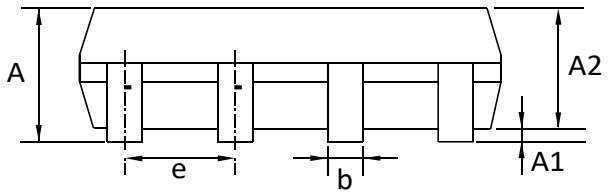
Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	1.35	0.05	1.35	0.38	0.17	4.80	5.80	3.80	1.27	0.50	1.04	0.30	0°
	Nom	1.55	0.10	1.40	-	-	4.90	6.00	3.90		0.60		0.40	-
	Max	1.65	0.15	1.50	0.51	0.25	5.00	6.20	4.00		0.80		0.50	8°

Note:

1. Both the package length and width do not include the mold FLASH.
2. Seating plane: Max. 0.25mm.

7.2 Package SOP8 208MIL





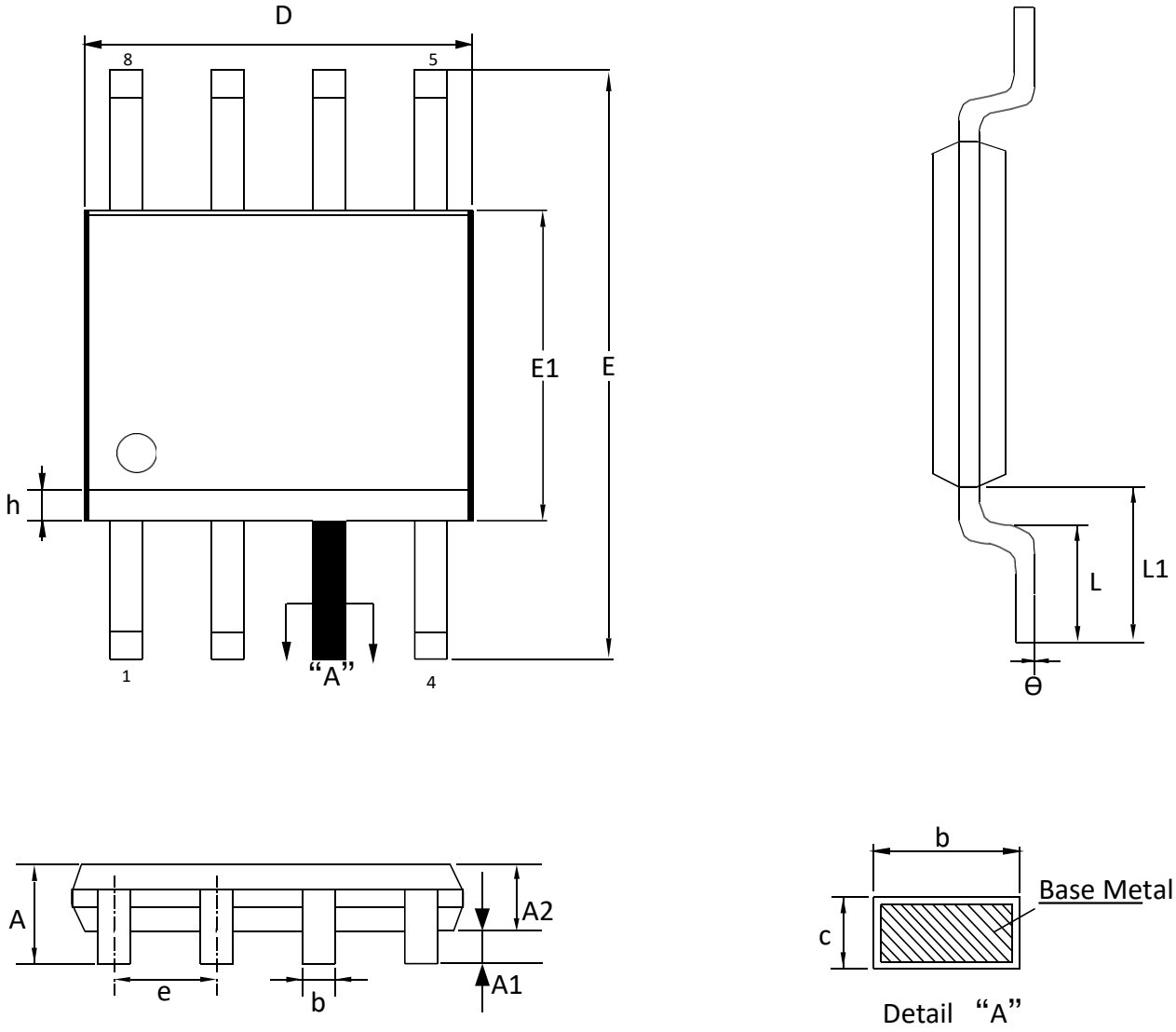
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	h	θ1	θ2	θ3
mm	Min	1.75	0.05	1.70	0.40	0.19	5.13	7.70	5.10	1.17	0.50	0.30			
	Nom	1.95	0.15	1.80	0.45	0.20	5.23	7.90	5.25	1.27	0.65	0.40	-	-	-
	Max	2.15	0.25	1.90	0.50	0.21	5.33	8.10	5.40	1.37	0.80	0.50			

Note:

3. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
4. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. ALL DIMENSIONS MEET JEDEC STANDRAD MS-012F

7.3 Package TSSOP8



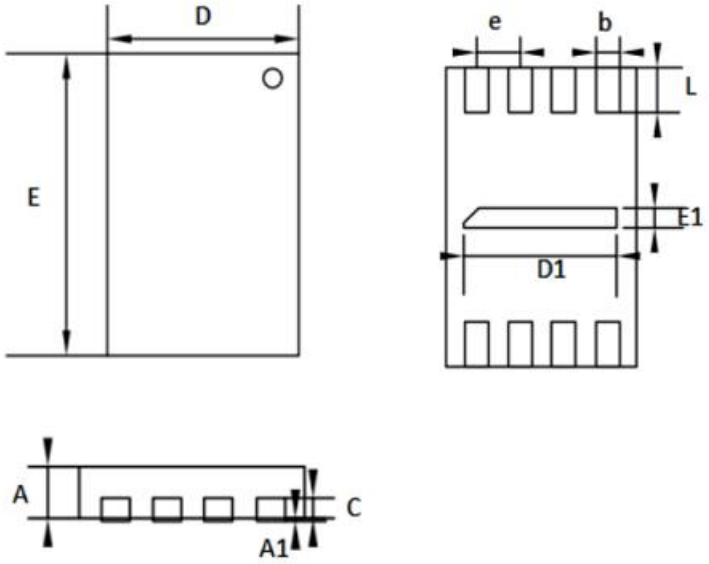
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min		0.05	0.8	0.19	0.09	2.90	6.20	4.30	0.65	0.45	1.00		0°
	Nom			1.00	-	-	3.00	6.40	4.40		0.60			-
	Max	1.2	0.15	1.05	0.30	0.20	3.10	6.60	4.50		0.75			8°

Note:

1. Both the package length and width do not include the mold FLASH.
2. Seating plane: Max. 0.25mm.

7.4 Package USON (2*3*0.45mm)



DFN2.0*3.0*0.45-8L POD			
	MIN	NOM	MAX
D	1.95	2.00	2.05
E	2.95	3.00	3.05
D1	1.55	1.60	1.65
E1	0.15	0.20	0.25
L	0.40	0.45	0.50
b	0.20	0.25	0.30
e	0.5BSC		
A	0.40	0.45	0.50
C	0.152REF		
A1	0.00	0.02	0.05

8. REVISION HISTORY

Version No	Description	Date
1.0	Initial Release	2021-03-20
1.1	Add USON2*3 package.	2022-01-08

IMPORTANT NOTICE

ZETTA Technology reserves the right to make changes, corrections, or modifications without further notice to any products or this document here in. ZETTA Technology does not assume any responsibility for use of any its products for any particular purpose, nor does ZETTA Technology assume any liability arising out of the application or use of any its products or circuits. ZETTA Technology does not convey any license under its patent rights or other rights nor the rights of others.